

# PDP11

## MAIN MEMORY CRAM TEST MD-11-DZKCD-A

EP-DZKCD-A-DL-A

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FICHE 1 OF 1

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The image displays a grid of 150 small data tables, arranged in 10 columns and 15 rows. Each table represents a memory test result for a specific location. The tables are organized into columns, with each column containing 15 individual test results. The data within each table is presented in a structured format, typically with a header row followed by several rows of numerical or alphanumeric values. The overall layout is a dense grid of test data, characteristic of a memory dump or test log for a PDP-11 system.

## IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZKCD-A-D  
PRODUCT NAME: MAIN MEMORY, JUMP AND CRAM TESTS ON MICRO-PROCESSOR  
DATE: MAY 1977  
MAINTAINER: DIAGNOSTICS  
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## 1. ABSTRACT

The function of the KMC11 diagnostics is to verify that the option operates according to specifications. The diagnostics verify that there are no malfunctions and that all operations of the KMC11 are correct in its environment.

Parameters must be set up to alert the diagnostics to the KMC11 configuration. These parameters are contained in the STATUS TABLE and are generated in two ways: 1) Manual Input - the operator answers questions. 2) Autosizing - the program determines the parameters automatically.

DZKCE tests the KMC11-AR micro-processor (M8204-YA) with low speed cram, or the KMC11 micro-processor (M8204). It performs jump tests on the micro-processor, and tests the CRAM and other unique functions of the M8204. If a KMC11-AR (M8200-YA) and line unit (M8201) are present, free-running tests are performed. These tests are skipped if a KMC (M8204) or no line-unit is present. The best test is with a line-unit installed. DZKCE can be used as a Heat Test Diagnostic by Manufacturing.

Currently there are four off line diagnostics that are to be run in sequence to insure that if an error should occur it will be detected at an early stage.

NOTE: Additional diagnostics may be added in the future.

The four diagnostics are:

1. DZKCC [REV] Basic W/R and Micro-processor tests
2. DZKCD [REV] jump and main memory tests
3. DZKCE [REV] DDCMP Line unit tests
4. DZKCF [REV] BITSTUFF Line unit tests
5. DZKCA [REV] KMC11 CPU MICRO-DIAGNOSTICS.

## 2. REQUIREMENTS

## 2.1 EQUIPMENT

Any PDP11 family CPU (except an LSI-11) with minimum 8k memory  
ASA 33 (or equivalent)  
KMC11-AR (M8200-YA) or an KMC11-A (M8204) with a KMC11-DA or a  
KMC11-FA

## 2.2 STORAGE

Program will use all BK of memory except where ABL and BOOTSTRAP LOADER reside. Locations 2100 thru 2300; contain the "STATUS TABLE" information which is generated at start of diagnostics by manual input (questions) or automatically (auto-sizing). This area is an overlay area and should not be altered by the operator.

## 3. LOADING PROCEDURE

### 3.1 METHOD

All programs are in absolute format and are loaded using the ABSOLUTE LOADER. NOTE: if the diagnostics are on a media such as DISK, MAGTAPE, DECTAPE, or CASSETTE; follow instructions for the monitor which has been provided on that specific media.

ABSOLUTE LOADER starting address #500

MEMORY # SIZE

4k	17
8k	37
12k	57
16k	77
20k	117
24k	137
28k	157

- 3.1.1 Place address of ABS loader into switch register.  
(also place 'HALT' SW up)
- 3.1.2 Depress 'LOAD ADDRESS' key on console and release.
- 3.1.3 Depress 'START KEY' on console and release (program should now be loading into CPU)

4. STARTING PROCEDURE

- a. Set switch register to 000200
- b. Depress 'LOAD ADDRESS' key and release
- c. Set SWR to zero for 'AUTO SIZING' or SWR bit0=1 for manual input (questions) or SWR bit7=1 to use existing parameters set up by a previous start or a previously run KMC11 diagnostic.
- d. Depress 'START KEY' and release. The program will type Maindec Name and program name (if this was the first start up of the program) and also the following:

MAP OF KMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
002100	160010	045310	177777	000000
002110	160020	045320	177777	000000

The program will type 'R' and proceed to run the diagnostic. The above is only an example. This would indicate the status table starting at add. 2100 in the program. In this example the table contains the information and status of two KMC11'S. THE STATUS TABLE MUST BE VERIFIED BY THE USER IF AUTO SIZING IS DONE. For information of status table see section B.4 for help.

If the diagnostic was started with SW00=1 indicating manual parameter input then the following shows an example of the questions asked and some example answers:

HOW MANY KMC11'S TO BE TESTED?1

01

CSR ADDRESS?160010

VECTOR ADDRESS?310

BR PRIORITY LEVEL? (4,5,6,7)?5

WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF

M8202 TYPE "2"?1

IS THE LOOP BACK CONNECTOR ON?Y

SWITCH PAC#1 (DOCMP LINE#)?377

SWITCH PAC#2 (BMB73 BOOT ADD)?377

Following the questions the status map is printed out as described above, the information in the map reflects the answers to the questions. If the diagnostic was started with SW00=0 and SW07=0 (AUTO-SIZING) then no questions are asked and only the status-map is printed out. If AUTO-SIZING is used the status information must be verified to be correct (match the hardware). if it does not match the hardware the diagnostic must be restarted with SW00=1 and the questions answered.

4.1 CONTROL SWITCH SETTINGS

SW	15	Set:	Halt on error
SW	14	Set:	Loop on current test
SW	13	Set:	Inhibit error print out
SW	12	Set:	Inhibit type out abell on error.
SW	11	Set:	Inhibit iterations. (quick pass)
SW	10	Set:	Escape to next test on error
SW	09	Set:	Loop with current data
SW	08	Set:	Catch error and loop on it
SW	07	Set:	Use previous status table.
SW	06	Set:	Halt in ROMCLK routine before clocking micro-processor
SW	05	Set:	Reserved
SW	04	Set:	Reserved
SW	03	Set:	Reselect KMC11's desired active
SW	02	Set:	Lock on selected test
SW	01	Set:	Restart program at selected test
SW	00	Set:	Build new status table from questions. (If SW07=0 and SW00=0 a new status table is built by auto-sizing)

Switch 06 and 08-15 are dynamic and can be changed as needed while the diagnostic is running. Switches 00-03 and switch 07 are static, and are used only on starting or restarting the diagnostic.

4.1.2 SWITCH REGISTER OPTIONS (at start up)

SW 01 RESTART PROGRAM AT SELECTED TEST. It is strongly suggested that at least one pass has been made before trying to select a test, the reason being is that the program has to clear areas and set up parameters. When this switch is used the diagnostic will ask "TEST NO.?" Answer by typing the number of the test desired and carriage return to begin execution at the selected test.

SW 02 LOCK ON SELECTED TEST. This switch when used with SW01 will cause the program to constantly loop on the selected test. Hitting any key on the console will let it advance to the next test and loop until a key is hit again. If SW02=0 when SW01 is used. The program will begin at the selected test and continue normal operations.

SW 03 RESELECT KMC11'S DESIRED ACTIVE. Please note that a message is typed out for setting the switch register equal to KMC11's active. this means if the system has four KMC11s; bits 00,01,02,03 will be set in loc 'KMACTV' from the switch register. Using this switch(SW03) alters that location; therefore if four KMC11s are in the system **\*\*\*DO NOT\*\*\*** set switches greater than SW 03 in the up position. this would be a fatal error. do not select more active KMC11s than there is information on in the status table.

METHOD: A: Load address 200  
 B: Start with SW 00=1  
 C: Program will type message  
 D: Set a switch for each KMC desired active.  
 EXAMPLE: If you have 4 KMC's but only want to run the first and the last set SWR bits 0 and 3 = 1. PRESS CONTINUE  
 E: Number (IF VALID) will be in data lights (excluding 11/05)  
 F: Set with any other switch settings desired. PRESS CONTINUE.

### 4.1.3 DYNAMIC SWITCHES

#### ERROR SWITCHES

- |    |       |                                       |
|----|-------|---------------------------------------|
| 1. | SW 12 | Delete print out/bell on error.       |
| 2. | SW 13 | Delete error printout.                |
| 3. | SW 15 | Halt on the error.                    |
| 4. | SW 08 | Goto beginning of the test(on error). |
| 5. | SW 10 | Goto next test(on error).             |

#### SCOPE SWITCHES

1. SW06 Halt in ROMCLK routine before clocking micro-processor instruction. This allows the operator to scope a micro-processor instruction in the static state before it is clocked. Hit continue to resume running.
2. SW09 (if enabled by 'SCOPI') on an error; If an '\*' is printed in front of the test no. (ex. \*TEST NO. 10 ) SW09 is incorporated in that test and therefore SW09 is usually the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enabled; and there is a HARD error (constant); SW08 is best. (SW14=1,0, SW10=0, SW09=0, SW08=1). for intermittent errors; SW14=1 will loop on test regardless of error or not error. (SW14=1, SW10=0, SW09=0, SW08=1,0)
3. SW11 Inhibit iterations.
4. SW14 Loop on current test.

### 4.2 STARTING ADDRESS

Starting address is at 000200 there are no other starting addresses for the KMC11 diagnostics. (See Section 4.0)

NOTE: If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly after all available KMC11's are tested the program will return to 'XXDP' or 'ACT-11'.

### 5. OPERATING PROCEDURE

When program is initially started messages as described in section 4.0 will be printed, and program will begin running the diagnostic



## 5.2 PROGRAM AND/OR OPERATOR ACTION

The typical approach should be

1. Halt on error (via SW 15=1) when ever an error occurs.
2. Clear SW 15.
3. Set SW 14: (loop on this test)
4. Set SW 13: (inhibit error print out)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTION of the test CAN BE DETERMINED.

## 6. ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW 13=0 and SW 12=0). in most cases additional information will be supplied in the error message to give the operator an indication of the error.

### 6.2 ERROR RECOVERY

If for some reason the KMC11 should 'HANG THE BUS' (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of cpu. If this should happen; look in location 'STSTNM' (address 1202) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the KMC11 was doing at the time of the error.

## 7. RESTRICTIONS

### 7.1 STARTING RESTRICTIONS

See section 4. (PLEASE)  
Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.

## 7.2 OPERATING RESTRICTIONS

The first time a KMC11 diagnostic is loaded into core and run the STATUS TABLE must be set up. This is done by manual input (SW00=1) or by autosizing (SW00=0 and SW07=0). Thereafter however the status table need not be setup by subsequent restarts or even loading the next KMC diagnostic because the STATUS TABLE is overlayed. The current parameters in the STATUS TABLE are used when SW07=1 on start up.

## 7.3 HARDWARE CONFIGURATION RESTRICTIONS

KMC11(MB204)- Jumper W1 must be in,

LINE UNIT(MB201)- Jumpers W1, W2, and W4 must be IN. Jumpers W3, and W5 must be OUT. SW8 of E26 must be in the ON POSITION.

LINE UNIT (MB202)- Jumper W1 must be in. SW8 of E26 must be in the OFF position.

## 8. MISCELLANEOUS

### 8.1 EXECUTION TIME

All KMC11 device diagnostics will give an 'END PASS' message (providing no errors and sw12=0) within 4 mins. This is assuming SW11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the PDP11 CPU configuration and the amount of memory in the system.

### 8.2 PASS COMPLETE

NOTE: EVERY time the program is started; the tests will run as if SW11 (delete iterations) was up (=1). This is to 'VERIFY NO HARD ERRORS' as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a 'QUICK PASS' until all KMC11's in system are tested. When the diagnostic has completed a pass the following is an example of the print out to be expected.

```
END PASS DZKCD CSR: 175000 VEC: 0300 PASSES: 000001
ERRORS: 000000
```

NOTE: The pass count and error counts are cummulative for each KMC11 that is running, and are set to zero only when the diagnostic is started. Therefore after an overnight run for example, the total passes and errors for each KMC11 since the diagnostic was started are reflected in PASSES: and ERRORS:.

8.4 KEY LOCATIONS

- Slpdr (1206) Contains the address where program will return when iteration count is reached or if loop on test is asserted.
- NEXT (1442) Contains the address of the next test to be performed.
- STSTNM (1202) Contains the number of the test now being performed.
- RUN (1500) The bit in 'RUN' always points to the KMC11 currently being tested. EXAMPLE: (RUN) 1500/0000000001000000 Means that KMC11 no.06 is the KMC11 now running.

KMCRO0-KMCR17  
KMST00-KMST17  
(2100)-(2300)

These locations contain the information needed to test up to 16 (decimal) KMC11s sequentially, they contain the CSR, VECTOR and STATUS concerning the configuration of each KMC11.

KMACTV (1470) Each bit set in this location indicates that the associated KMC11 will be tested in turn. EXAMPLE: (KMACTV) 1470/0000000000011111 means that KMC11 no. 00,01,02,03,04 will be tested. EXAMPLE: (KMACTV) 1470/000000000010001 Means that KMC11 no. 00,04 will be tested.

KMCSR (2066) Contains the CSR of the current KMC11 under test.

8.4A 'STATUS TABLE' (2100-2300)

The table is filled by AUTO SIZING or by the manual parameter input (questions) as described previously. Also if desired by user; the locations may be altered by hand (toggled in) to suit the specific configuration.

The example status map shown below contains information for two KMC11'S. the table can contain up to 16 KMC11'S. Following the map is a description of the bits for each map entry

MAP OF KMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
002100	160010	045310	177777	000000
002110	160020	016320	000000	000000

Each map entry contains 4 words which contain the status information for 1 KMC11. The PC shows where in core memory the first of the 4 words is. In the example above the first KMC'S status is in locations, 2100, 2102, 2104, and 2106. The second KMC status is located at 2110, 2112, 2114, and 2116. The information contained in each 4 word entry is defined as follows:

CSR: Contains KMC11 CSR address

STAT1: BITS 00-08 IS KMC11 VECTOR ADDRESS  
 BIT14=1 TURNAROUND CONNECTOR IS ON  
 BIT14=0 NO TURNAROUND CONNECTOR  
 BIT13=0 LINE UNIT IS AN M8201  
 BIT13=1 LINE UNIT IS AN M8202  
 BIT12=1 NO LINE UNIT  
 BITS 09-11 IS KMC11 BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)  
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)

STAT3: BIT0=1 PERFORM FREE RUNNING TESTS ON KMC  
 (must be set manually. SEE TEST 50)

## 8.5 METHOD OF AUTO SIZING

### 8.5.1 FINDING THE CONTROL STATUS REGISTER.

The auto-sizing routine finds a KMC11 as follows: It starts at address 160000 and tests all address in increments of 10 up to and including address 167760. If the address does not time out, the following is done, the first CRAM address is written to a 125252 then it is read back. If it contains a -1 or 125252 KMC11 has been found, if not, the address is updated by 10 and the search continues. A -1 indicates a KMC11 with no CRAM, and a 125252 indicates a KMC11 with CRAM. Further tests are performed at this point to determine which line unit, if any, is installed, if a loop-back connector is installed and various switch settings on the line unit. THIS IS WHY THE STATUS TABLE MUST BE VERIFIED BY THE USER AND IF ANY OF THE INFORMATION DOES NOT AGREE WITH THE HARDWARE THE DIAGNOSTIC MUST BE RESTARTED AND THE QUESTIONS MUST BE ANSWERED. All KMC11's in the system will be found by the auto-sizer. If it does not find a KMC11 the diagnostic must be restarted and the questions answered.

### 8.5.2 FINDING THE VECTOR AND BR LEVEL

The vector area (address 300-776) is filled with the instruction IOT and '+2' (next address). The processor status is started at 7 and the KMC is programmed to interrupt. The PS is lowered by 1 until the KMC interrupts, a e-lay is made and if no interrupt occurs at PS level 3 (because of a bad KMC11) the program assumes vector address 300 at BR level 5 and the problem should be fixed in the diagnostic. Once the problem is fixed; the program should be re-setup again to get correct vector. If an interrupt occurred; the address to which the KMC11 interrupted to is picked up and reported as the vector. NOTE: if the vector reported is not the vector set up by you; there is a problem and AUTO SIZING should not be done.

## 8.5 SOFTWARE SWITCH REGISTER

If the diagnostic is run on an 11/04 or other CPU without a switch register then a software switch register is used to allow user the same switch options as described previously. If the hardware switch register does not exist or if one does and it contains all ones (177777) this software switch register is used.

Control:

To obtain control at any allowable time during execution of the diagnostic the operator types a CTRL G on the console terminal keyboard. As soon as the CTRL G is recognized, by the diagnostic, the following message will be displayed:

SWR=XXXXXX NEW?

Where XXXXXX is the current contents of the software switch register in octal. The software control routine will then await operator action. At which time the operator is required to type one or more of the legal characters: 1) 0 - 7, 2) line feed(<LF>), 3) carriage return(<CR>), or 4) control-U (CTRL U). No check is made for legality. If the input character is not a <LF>, <CR>, or CTRL U it is assumed to be an octal digit.

To change the contents of the SSR the operator simply types the new desired value in octal - leading zeros need not be typed. And terminates the input string with a <CR> or <LF> depending on the program action desired as described below. The input value will be truncated to the last 6 digits typed. At least one digit must be typed on any given input string prior to the terminator before a change to the SSR will occur.

When the input string is terminated with a <CR> the diagnostic will continue execution from the point at which it was interrupted. If a <CR> is the only thing typed the program will continue without changing the SSR. The <LF> differs from the <CR> by restarting the program as if it were restarted at address 200.

If a CTRL U is typed at any point in the input string prior to the terminator the input value will be disregarded and the prompt displayed (SWR = XXXXXX NEW?).

To set the SSR for the starting switches, first load the diagnostic, then hit CTRL G, then start the diagnostic.



APT/ACT/XXDP/SLIDE

\*\*\*\*\*

THIS DIAGNOSTIC IS APT/ACT/XXDP/SLIDE COMPATIBLE USER WOULD BE ABLE TO RUN IT UNDER APT/ACT/XXDP ENVIRONMENT.

NOTE: FOR MANUFACTURING PURPOSE ONLY ITS DESCRIBED HOW TO RUN UNDER APT ENVIRONMENT.

\*\*\*\*\*

ETABLE SETTING FOR APT TO RUN UNDER APT

\*\*\*\*\*

FIRST PASS TIME:

LONGEST TEST TIME:

ADDITIONAL TEST TIME:

ALL THE ABOVE PARAMETERS ARE DEPENDENT ON PARTICULAR DIAGNOSTICS AND SHOULD BE LOADED AT THE TIME OF SETTING ETABLE.THERE IS NO DEFAULT TIME SET UP.

SOFTWARE ENVIRONMENT:001 ENVIRONMENT MODE:200

SWITCH 1:-SHOULD BE USED AS NORMAL SWITCH REGISTER.

SWITCH 2:-NOT USED.

CPU OPTIONS:-NOT USED.

MEMORY TYPE 1:-BITS<2:4>:=BITS <12:14> OF STAT1 OF DEV:0.

MAXIMUM ADDRESS:-BITS<17:19>:=BITS<12:14> OF STAT1 OF DEV:1

          BITS<2:4>:=BITS <12:14> OF STAT1 OF DEV:2

          BITS<10:12>:=BITS<12:14> OF STAT1 OF DEV:3

IN THE SAME MANNER

MEMORY TYPE 2 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE 4,5,6,7.

MEMORY TYPE 3 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE 8,9,10,11.

MEMORY TYPE 4 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE 12,13,14,15.

INTERRUPT VECTOR 1:FIRST DEVICE RECEIVE VECTOR.

REST OF THE DEVICE(KMC'S) VECTOR SHOULD BE SET UP SEQUENTIALLY  
IN INCREMENTS OF 10.

BUS PRIORITY:KMC'S PRIORITY(SHOULD BE SAME FOR ALL KMC'S UNDER  
TEST).

INTERRIPT VECTOR 2:NOT USED.

BUS PRIORITY:NOT USED.

BASE ADDRESS:FIRST DEVICE CSR ADDRESS.

REST SHOULD FOLLOW SEQUENTIALLY

IN INCREMENTS OF 10.

DEVICE MAP:AS DESCRIBED IN APT MANUAL.

CONTROLLER SPECIFIC CODE 1:-NO. OF DEVICES UNDER TEST.

CONTROLLER SPECIFIC CODE 2:-NOT USED.

DEVICE DESCRIPTOR WORD 0:STAT2 OF FIRST DEVICE.

. . .

. . .

TO

. . .

. . .

DEVICE DESCRIPTOR WORD 15:STAT2 OF 16TH DEVICE.(KMC)

MAINDEC-11-DZKCD

002

DECDOC VER 00.04 12-MAY-77 18:44 PAGE 01 PAGE: 0016

DOCUMENT  
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MAINDEC-11-DZKCD  
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- 2191 \*\*\*\*\* TEST 1 \*\*\*\*\*  
 TEST OF BR RIGHT SHIFT  
 VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION  
 SHIFTS THE RESULTING BR DATA RIGHT ONCE.
  
- 2233 \*\*\*\*\* TEST 2 \*\*\*\*\*  
 IOP CROM WRITE/READ TEST  
 FLOAT A 1 THROUGH EACH CROM LOCATION
  
- 2267 \*\*\*\*\* TEST 3 \*\*\*\*\*  
 IOP CROM WRITE/READ TEST  
 FLOAT A 0 THROUGH EACH CROM LOCATION
  
- 2304 \*\*\*\*\* TEST 4 \*\*\*\*\*  
 IOP CROM DUAL ADDRESSING TEST  
 WRITE EACH ADDRESS INTO ITSELF, READ EACH  
 ADDRESS TO VERIFY CORRECT ADDRESSING
  
- 2350 \*\*\*\*\* TEST 5 \*\*\*\*\*  
 IOP CROM READ TEST  
 THIS TEST WRITES THE CROM WITH THE CROM MICRO-CODE MAP  
 THEN READS IT BACK AND COMPARES EACH ADDRESS WITH THE  
 DUPLICATE OF THE CROM MICRO-CODE.
  
- 2387 \*\*\*\*\* TEST 6 \*\*\*\*\*  
 IOP MAIN MEMORY TEST  
 FLOAT A 1 THROUGH ALL MAIN MEMORY LOCATIONS
  
- 2433 \*\*\*\*\* TEST 7 \*\*\*\*\*  
 IOP MAIN MEMORY TEST  
 FLOAT A 0 THROUGH ALL MAIN MEMORY LOCATIONS
  
- 2481 \*\*\*\*\* TEST 10 \*\*\*\*\*  
 IOP MAIN MEMORY DUAL ADDRESSING TEST  
 LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS  
 READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING
  
- 2549 \*\*\*\*\* TEST 11 \*\*\*\*\*  
 IOP MAR TEST  
 PERFORM DUAL ADDRESSING TEST  
 USING MAR AUTO-INC FEATURE

- 2589 \*\*\*\*\* TEST 12 \*\*\*\*\*  
IOP (CRAM) OOT BITS TEST  
LOAD MAR WITH A 0 INC MAR UNTIL IT OVERFLOWS (2000 TIMES)  
VERIFY THAT IBUS\* 10 BITS IS SET ONLY WHEN MAR BIT 8 IS A ONE  
AND THAT IBUS\* 10 BIT6 IS SET ON MAR OVERFLOW(2000)
- 2650 \*\*\*\*\* TEST 13 \*\*\*\*\*  
CRAM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.  
PERFORM THE JUMP INSTRUCTION  
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,  
THEN PORT4 CONTAINS A 37
- 2711 \*\*\*\*\* TEST 14 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.  
PERFORM THE JUMP INSTRUCTION  
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,  
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
THEN PORT4 WILL CONTAIN A 37
- 2769 \*\*\*\*\* TEST 15 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.  
SET THE C BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,  
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
THEN PORT4 WILL CONTAIN A 37
- 2830 \*\*\*\*\* TEST 16 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.  
SET THE Z BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,  
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
THEN PORT4 WILL CONTAIN A 37
- 2891 \*\*\*\*\* TEST 17 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,  
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL

THEN PORT4 WILL CONTAIN A 37

- 2952 \*\*\*\*\* TEST 20 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,  
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
THEN PORT4 WILL CONTAIN A 37
- 3013 \*\*\*\*\* TEST 21 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,  
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
THEN PORT4 WILL CONTAIN A 37
- 3074 \*\*\*\*\* TEST 22 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,  
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
THEN PORT4 WILL CONTAIN A 37
- 3135 \*\*\*\*\* TEST 23 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
- 3140 BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,  
THEN PORT4 CONTAINS A 37
- 3196 \*\*\*\*\* TEST 24 \*\*\*\*\*  
CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,  
THEN PORT4 CONTAINS A 37



3257 \*\*\*\*\* TEST 25 \*\*\*\*\*  
 CRAM TEST OF JUMP(I) ON BR0 SET MICRO-PROCESSOR INSTRUCTION.  
 CLEAR THE BR0 BIT, PERFORM THE JUMP INSTRUCTION,  
 VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
 IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
 BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
 THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
 THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,  
 THEN PORT4 CONTAINS A 37

3318 \*\*\*\*\* TEST 26 \*\*\*\*\*  
 CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.  
 CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,  
 VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
 IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
 BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
 THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
 THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,  
 THEN PORT4 CONTAINS A 37

3379 \*\*\*\*\* TEST 27 \*\*\*\*\*  
 CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.  
 CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,  
 VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
 IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
 BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
 THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
 THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,  
 THEN PORT4 CONTAINS A 37

3440 \*\*\*\*\* TEST 30 \*\*\*\*\*  
 CRAM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.  
 CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,  
 VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
 IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
 BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
 THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
 THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,  
 THEN PORT4 CONTAINS A 37

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```

.TITLE MAINDEC-11-DZKCD
.*COPYRIGHT (C) 1976
.*DIGITAL EQUIPMENT CORP.
.*MAYNARD, MASS. 01754
.*
.*PROGRAM BY DINESH GORADIA
.*
.*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
.*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
.*

```

```

.*MAINDEC-11-DZKCD KMC11 REMOTE CROM, JUMP TESTS
.*COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
.*-----

```

```

;STARTING PROCEDURE
;LOAD PROGRAM
;LOAD ADDRESS 000200
;SWR=0 AUTOSIZE KMC11
;SM07=1 USE CURRENT KMC11 PARAMETERS
;SM00=1 INPUT NEW KMC11 PARAMETERS
;PRESS START
;PROGRAM WILL TYPE "MAINDEC-11-DZKCD KMC11 REMOTE CROM, JUMP TESTS"
;PROGRAM WILL TYPE STATUS MAP
;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
;AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
;AND THEN RESUME TESTING
;SUBSEQUENT RESTARTS WILL NOT TYPE PROGRAM TITLE

```

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.SBTTL BASIC DEFINITIONS

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```

.*INITIAL ADDRESS OF THE STACK POINTER *** 1200 ***
001200 STACK= 1200
.EQUIV EMT,ERROR ;;BASIC DEFINITION OF ERROR CALL
.EQUIV IOT,SCOPE ;;BASIC DEFINITION OF SCOPE CALL

```

```

.*MISCELLANEOUS DEFINITIONS
000011 HT= 11 ;;CODE FOR HORIZONTAL TAB
000012 LF= 12 ;;CODE FOR LINE FEED
000015 CR= 15 ;;CODE FOR CARRIAGE RETURN
000200 CRLF= 200 ;;CODE FOR CARRIAGE RETURN-LINE FEED
177776 PS= 177776 ;;PROCESSOR STATUS WORD
.EQUIV PS,PSW
177774 STKLM= 177774 ;;STACK LIMIT REGISTER
177772 PIRQ= 177772 ;;PROGRAM INTERRUPT REQUEST REGISTER
177570 DSWR= 177570 ;;HARDWARE SWITCH REGISTER
177570 DISP= 177570 ;;HARDWARE DISPLAY REGISTER

```

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.*GENERAL PURPOSE REGISTER DEFINITIONS
000000 R0= %0 ;;GENERAL REGISTER
000001 R1= %1 ;;GENERAL REGISTER
000002 R2= %2 ;;GENERAL REGISTER

```

57	000003	R3=	%3	:: GENERAL REGISTER
58	000004	R4=	%4	:: GENERAL REGISTER
59	000005	R5=	%5	:: GENERAL REGISTER
60	000006	R6=	%6	:: GENERAL REGISTER
61	000007	R7=	%7	:: GENERAL REGISTER
62	000006	SP=	%6	:: STACK POINTER
63	000007	PC=	%7	:: PROGRAM COUNTER

.\*PRIORITY LEVEL DEFINITIONS

65		PRO=	0	:: PRIORITY LEVEL 0
66	000000	PR0=	0	:: PRIORITY LEVEL 0
67	000040	PR1=	40	:: PRIORITY LEVEL 1
68	000100	PR2=	100	:: PRIORITY LEVEL 2
69	000140	PR3=	140	:: PRIORITY LEVEL 3
70	000200	PR4=	200	:: PRIORITY LEVEL 4
71	000240	PR5=	240	:: PRIORITY LEVEL 5
72	000300	PR6=	300	:: PRIORITY LEVEL 6
73	000340	PR7=	340	:: PRIORITY LEVEL 7

.\*"SWITCH REGISTER" SWITCH DEFINITIONS

75		SW15=	100000	
76	100000	SW15=	100000	
77	040000	SW14=	40000	
78	020000	SW13=	20000	
79	010000	SW12=	10000	
80	004000	SW11=	4000	
81	002000	SW10=	2000	
82	001000	SW09=	1000	
83	000400	SW08=	400	
84	000200	SW07=	200	
85	000100	SW06=	100	
86	000040	SW05=	40	
87	000020	SW04=	20	
88	000010	SW03=	10	
89	000004	SW02=	4	
90	000002	SW01=	2	
91	000001	SW00=	1	
92		.EQUIV	SW09, SW9	
93		.EQUIV	SW08, SW8	
94		.EQUIV	SW07, SW7	
95		.EQUIV	SW06, SW6	
96		.EQUIV	SW05, SW5	
97		.EQUIV	SW04, SW4	
98		.EQUIV	SW03, SW3	
99		.EQUIV	SW02, SW2	
100		.EQUIV	SW01, SW1	
101		.EQUIV	SW00, SW0	

.\*DATA BIT DEFINITIONS (BIT00 TO BIT15)

103		BIT15=	100000	
104	100000	BIT15=	100000	
105	040000	BIT14=	40000	
106	020000	BIT13=	20000	
107	010000	BIT12=	10000	
108	004000	BIT11=	4000	
109	002000	BIT10=	2000	
110	001000	BIT09=	1000	
111	000400	BIT08=	400	
112	000200	BIT07=	200	

## BASIC DEFINITIONS

```

113      000100      BIT06= 100
114      000040      BIT05= 40
115      000020      BIT04= 20
116      000010      BIT03= 10
117      000004      BIT02= 4
118      000002      BIT01= 2
119      000001      BIT00= 1
120      .EQUIV BIT09,BIT9
121      .EQUIV BIT08,BIT8
122      .EQUIV BIT07,BIT7
123      .EQUIV BIT06,BIT6
124      .EQUIV BIT05,BIT5
125      .EQUIV BIT04,BIT4
126      .EQUIV BIT03,BIT3
127      .EQUIV BIT02,BIT2
128      .EQUIV BIT01,BIT1
129      .EQUIV BIT00,BIT0
130
131      ;#BASIC "CPU" TRAP VECTOR ADDRESSES
132      000004      ERRVEC= 4      ; TIME OUT AND OTHER ERRORS
133      000010      RESVEC= 10     ; RESERVED AND ILLEGAL INSTRUCTIONS
134      000014      TBITVEC=14     ; "T" BIT
135      000014      TRTVEC= 14     ; TRACE TRAP
136      000014      BPTVEC= 14     ; BREAKPOINT TRAP (BPT)
137      000020      IOTVEC= 20     ; INPUT/OUTPUT TRAP (IOT) **SCOPE**
138      000024      PWRVEC= 24     ; POWER FAIL
139      000030      EMTVEC= 30     ; EMULATOR TRAP (EMT) **ERROR**
140      000034      TRAPVEC=34     ; "TRAP" TRAP
141      000060      TKVEC= 60      ; TTY KEYBOARD VECTOR
142      000064      TPVEC= 64      ; TTY PRINTER VECTOR
143      000240      PIRQVEC=240    ; PROGRAM INTERRUPT REQUEST VECTOR
144
145
146
147
148      ; INSTRUCTION DEFINITIONS
149      ;-----
150
151      005746      PUSH1SP=5746    ; DECREMENT PROCESSOR STACK 1 WORD
152      005726      POP1SP=5726    ; INCREMENT PROCESSOR STACK 1 WORD
153      010046      PUSHRO=10046    ; SAVE R0 ON STACK
154      012600      POPRO=12600    ; RESTORE R0 FROM STACK
155      024646      PUSH2SP=24646  ; DECREMENT STACK TWICE
156      022626      POP2SP=22626  ; INCREMENT STACK TWICE
157      .EQUIV EMT,HLT ; BASIC DEFINITION OF ERROR CALL
158
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160

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TRAPCATCHER FOR UNEXPECTED INTERRUPTS

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:*****
-----
: TRAPCATCHER FOR ILLEGAL INTERRUPTS
: THE STANDARD "TRAP CATCHER" IS PLACED
: BETWEEN ADDRESS 0 TO ADDRESS 776.
: IT LOOKS LIKE "PC+2 HALT".
-----
:*****

.=0
000000 000000 000000
      .WORD 0,0
: STANDARD INTERRUPT VECTORS
-----

.=20
000020 004134 ; $SCOPE ; SCOPE LOOP HANDLER.
000022 000340 PR7 ; SERVICE AT LEVEL 7.
000024 007126 $PWDRN ; POWER FAIL HANDLER
000026 000340 PR7 ; SERVICE AT LEVEL 7
000030 006512 $ERROR ; ERROR HANDLER
000032 000340 PR7 ; SERVICE AT LEVEL 7
000034 006414 $TRAP ; GENERAL HANDLER DISPATCH SERVICE
000036 000340 PR7 ; SERVICE AT LEVEL 7

.SBTTL ACT11 HOOKS

:*****
: HOOKS REQUIRED BY ACT11
      $SVPC= ; SAVE PC
      .=46
      $ENDAD ; ;1)SET LOC.46 TO ADDRESS OF $ENDAD IN .SEOP
      .=52
      .WORD BIT14 ; ;2)SET LOC.52 TO BIT14
      .=$SVPC ; ; RESTORE PC
      ; BIT14=1 PROGRAM EXECUTION TIME
      ; IS MEMORY SIZE DEPENDENT

.=174
DISPREG:0 ; SOFTWARE DISPLAY REGISTER
SWREG: 0 ; SOFTWARE SWITCH REGISTER

.=200
000200 000137 002402 JMP .START ; GO TO START OF PROGRAM

.=1000
001000 005200 040515 047111 MTITLE: .ASCII <200><12>/MAINDEC-11-DZKCD/<200>
(2) 001023 113 041515 030461 .ASCII /KMC11 REMOTE CROM, JUMP TESTS/<200>

DSWR = 177570
DDISP = 177570

```

210  
211  
212  
213  
214  
215  
216  
217 001200  
218 001200 000000  
219 001202 000  
220 001203 000  
221 001204 000000  
222 001206 000000  
223 001210 000000  
224 001212 000000  
225 001214 000  
226 001215 001  
227 001216 000000  
228 001220 000000  
229 001222 000000  
230 001224 000000  
231 001226 000000  
232 001230 000000  
233 001232 000000  
234 001234 000  
235 001235 000  
236 001236 000000  
237 001240 177570  
238 001242 177570  
239 001244 177560  
240 001246 177562  
241 001250 177564  
242 001252 177566  
243 001254 000  
244 001255 002  
245 001256 012  
246 001257 000  
247 001260 000000  
248  
249 001262 000000  
250 001264 000000  
251 001266 000000  
252 001270 000000  
253 001272 000000  
254 001274 000000  
255 001276 000000  
256 001300 000000  
257 001302 000000  
258 001304 000000  
259 001306 000000  
260 001310 000000  
261 001312 077  
262 001313 015  
263 001314 000012  
264  
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.SBTTL COMMON TAGS

\*\*\*\*\*  
\*THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS  
\*USED IN THE PROGRAM.

SCMTAG: .=1200

.WORD 0  
STSTNM: .BYTE 00  
SERFLG: .BYTE 00  
SICNT: .WORD 00  
SLPADR: .WORD 00  
SLPERR: .WORD 00  
SERTTL: .WORD 00  
SITEMB: .BYTE 00  
SERMAX: .BYTE 1  
SERAPC: .WORD 00  
SGOODR: .WORD 00  
SBOOR: .WORD 00  
SGDDAT: .WORD 00  
SBDAT: .WORD 00  
SAUTOB: .BYTE 00  
SINTAG: .BYTE 00  
SWR: .WORD DSWR  
DISPLAY: .WORD DDISP  
\$TKS: 177560  
\$TKB: 177562  
\$TPS: 177564  
\$TPB: 177566  
\$NULL: .BYTE 0  
\$FILLS: .BYTE 2  
\$FILLC: .BYTE 12  
\$TPFLG: .BYTE 0  
\$REGAD: .WORD 0  
\$REG0: .WORD 0  
\$REG1: .WORD 0  
\$REG2: .WORD 0  
\$REG3: .WORD 0  
\$REG4: .WORD 0  
\$REG5: .WORD 0  
\$TMP0: .WORD 0  
\$TMP1: .WORD 0  
\$TMP2: .WORD 0  
\$TMP3: .WORD 0  
\$TMP4: .WORD 0  
\$TIMES: 0  
\$QUES: .ASCII /?/  
\$CRLF: .ASCII <15>  
\$LF: .ASCII <12>

;; START OF COMMON TAGS

;; CONTAINS THE TEST NUMBER  
;; CONTAINS ERROR FLAG  
;; CONTAINS SUBTEST ITERATION COUNT  
;; CONTAINS SCOPE LOOP ADDRESS  
;; CONTAINS SCOPE RETURN FOR ERRORS  
;; CONTAINS TOTAL ERRORS DETECTED  
;; CONTAINS ITEM CONTROL BYTE  
;; CONTAINS MAX. ERRORS PER TEST  
;; CONTAINS PC OF LAST ERROR INSTRUCTION  
;; CONTAINS ADDRESS OF 'GOOD' DATA  
;; CONTAINS ADDRESS OF 'BAD' DATA  
;; CONTAINS 'GOOD' DATA  
;; CONTAINS 'BAD' DATA  
;; RESERVED--NOT TO BE USED  
;; AUTOMATIC MODE INDICATOR  
;; INTERRUPT MODE INDICATOR  
;; ADDRESS OF SWITCH REGISTER  
;; ADDRESS OF DISPLAY REGISTER  
;; TTY KBD STATUS  
;; TTY KBD BUFFER  
;; TTY PRINTER STATUS REG. ADDRESS  
;; TTY PRINTER BUFFER REG. ADDRESS  
;; CONTAINS NULL CHARACTER FOR FILLS  
;; CONTAINS # OF FILLER CHARACTERS REQUIRED  
;; INSERT FILL CHARS. AFTER A "LINE FEED"  
;; "TERMINAL AVAILABLE" FLAG (BIT<07>=0=YES)  
;; CONTAINS THE ADDRESS FROM  
;; WHICH (\$REG0) WAS OBTAINED  
;; CONTAINS ((SREGAD)+0)  
;; CONTAINS ((SREGAD)+2)  
;; CONTAINS ((SREGAD)+4)  
;; CONTAINS ((SREGAD)+6)  
;; CONTAINS ((SREGAD)+10)  
;; CONTAINS ((SREGAD)+12)  
;; USER DEFINED  
;; USER DEFINED  
;; USER DEFINED  
;; USER DEFINED  
;; USER DEFINED  
;; MAX. NUMBER OF ITERATIONS  
;; QUESTION MARK  
;; CARRIAGE RETURN  
;; LINE FEED

\*\*\*\*\*  
.SBTTL APT MAILBOX-ETABLE



Line	Address	Value	Field Name	Description
266			SMAIL:	APT MAILBOX
267			SMASCTY: .WORD	MESSAGE TYPE CODE
268			SMFATAL: .WORD	FATAL ERROR NUMBER
269	001316		SMTESTN: .WORD	TEST NUMBER
270	001316	000000	SMSPASS: .WORD	PASS COUNT
271	001320	000000	SMDEVCT: .WORD	DEVICE COUNT
272	001322	000000	SMUNIT: .WORD	I/O UNIT NUMBER
273	001324	000000	SMMSGAD: .WORD	MESSAGE ADDRESS
274	001326	000000	SMMSGLG: .WORD	MESSAGE LENGTH
275	001330	000000	SETABLE:	APT ENVIRONMENT TABLE
276	001332	000000	SENV: .BYTE	ENVIRONMENT BYTE
277	001334	000000	SENVH: .BYTE	ENVIRONMENT MODE BITS
278	001336	002	SSWREG: .WORD	APT SWITCH REGISTER
279	001337	000	SUSWR: .WORD	USER SWITCHES
280	001340	000000	SCPUOP: .WORD	CPU TYPE, OPTIONS
281	001342	000000		BITS 15-11=CPU TYPE
282	001344	000000		11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
283				11/70=06, P00=07, Q=10
284				BIT 10=REAL TIME CLOCK
285				BIT 9=FLOATING POINT PROCESSOR
286				BIT 8=MEMORY MANAGEMENT
287				;; HIGH ADDRESS, M.S. BYTE
288				;; MEM. TYPE BLK#1
289				MEM. TYPE BYTE -- (HIGH BYTE)
290	001346	000		900 NSEC CORE=001
291	001347	000		300 NSEC BIPOLAR=002
292				500 NSEC MOS=003
293				;; HIGH ADDRESS, BLK#1
294				MEM. LAST ADDR.=3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
295				;; HIGH ADDRESS, M.S. BYTE
296	001350	000000		;; MEM. TYPE, BLK#2
297				;; MEM. LAST ADDRESS, BLK#2
298	001352	000		;; HIGH ADDRESS, M.S. BYTE
299	001353	000		;; MEM. TYPE, BLK#3
300	001354	000000		;; MEM. LAST ADDRESS, BLK#3
301	001356	000		;; HIGH ADDRESS, M.S. BYTE
302	001357	000		;; MEM. TYPE, BLK#4
303	001360	000000		;; MEM. LAST ADDRESS, BLK#4
304	001362	000		;; HIGH ADDRESS, M.S. BYTE
305	001363	000		;; MEM. TYPE, BLK#4
306	001364	000000		;; MEM. LAST ADDRESS, BLK#4
307	001366	000000		;; INTERRUPT VECTOR#1, BUS PRIORITY#1
308	001370	000000		;; INTERRUPT VECTOR#2, BUS PRIORITY#2
309	001372	000000		;; BASE ADDRESS OF EQUIPMENT UNDER TEST
310	001374	000000		;; DEVICE MAP
311	001376	000000		;; CONTROLLER DESCRIPTION WORD#1
312	001400	000000		;; CONTROLLER DESCRIPTION WORD#2
313	001402	000000		;; DEVICE DESCRIPTOR WORD#0
314	001404	000000		;; DEVICE DESCRIPTOR WORD#1
315	001406	000000		;; DEVICE DESCRIPTOR WORD#2
316	001410	000000		;; DEVICE DESCRIPTOR WORD#3
317	001412	000000		;; DEVICE DESCRIPTOR WORD#4
318	001414	000000		;; DEVICE DESCRIPTOR WORD#5
319	001416	000000		;; DEVICE DESCRIPTOR WORD#6
320	001420	000000		;; DEVICE DESCRIPTOR WORD#7
321	001422	000000		;; DEVICE DESCRIPTOR WORD#8

APT MAILBOX-ETABLE

322 001424 000000  
323 001426 000000  
324 001430 000000  
325 001432 000000  
326 001434 000000  
327 001436 000000  
328 001440 000000

SDOW9: .WORD ADDR9 ;: DEVICE DESCRIPTOR WORD#9  
SDOW10: .WORD ADDR10 ;: DEVICE DESCRIPTOR WORD#10  
SDOW11: .WORD ADDR11 ;: DEVICE DESCRIPTOR WORD#11  
SDOW12: .WORD ADDR12 ;: DEVICE DESCRIPTOR WORD#12  
SDOW13: .WORD ADDR13 ;: DEVICE DESCRIPTOR WORD#13  
SDOW14: .WORD ADDR14 ;: DEVICE DESCRIPTOR WORD#14  
SDOW15: .WORD ADDR15 ;: DEVICE DESCRIPTOR WORD#15

331 001442

SETEND:

PROGRAM CONTROL PARAMETERS

336 001442 000000  
337 001444 000000

NEXT: .WORD 0 ;: ADDRESS OF NEXT TEST TO BE EXECUTED  
LOCK: .WORD 0 ;: ADDRESS FOR LOCK CURRENT DATA

PROGRAM VARIABLES

341 001446 000000  
342 001450 000000  
343 001452 000000  
344 001454 000000  
345 001456 000000  
346 001460 000000  
347 001462 000000  
348 001464 000001  
349 001466 000000  
350 001470 000001  
351 001472 000001  
352 001474 000001  
353 001476 000001  
354 001500 000000

STRTSM: .WORD 0 ;: SWITCHES AT START OF PROGRAM  
STAT: .WORD 0 ;: KM STATUS WORD STORAGE  
CLKX: .WORD 0  
MASKX: .WORD 0  
SAVSP: .WORD 0 ;: STACK POINTER STORAGE  
SAVPC: .WORD 0 ;: PROGRAM COUNTER STORAGE  
ZERO: .WORD 0  
ONE: .WORD 1  
MEMLIM: .WORD 0 ;: HIGHEST LOCATION FOR NPR'S  
KMACTV: .BLKW 1 ;: KMC11 SELECTED ACTIVE  
KMINUM: .BLKW 1 ;: OCTAL NUMBER OF KMC11'S  
SAVACT: .BLKW 1 ;: ORIGINAL ACTIVE DEVICES.  
SAVNUM: .BLKW 1 ;: WORKABLE NUMBER.  
RUN: .WORD 0 ;: POINTER TO RUNNING DEVICES

356 001502 002072  
357 001504 002276

CREAM: .WORD KM.MAP-6 ;: TABLE POINTER  
MILK: .WORD CNT.MAP-4 ;: TABLE POINTER

PROGRAM CONTROL FLAGS

361 001506 000  
362 001510 001510  
363 001511 000  
364 001511 000

INIFLG: .BYTE 0 ;: PROGRAM INITIALIZING FLAG  
LOKFLG: .BYTE 0 ;: LOCK ON CURRENT TEST FLAG  
QV.FLG: .BYTE 0 ;: QUICK VERIFY FLAG  
ON FIRST PASS OF EACH KMC11 ITERATIONS WILL BE SUPPRES  
.EVEN

365  
366

ERROR POINTER TABLE

.SBTTL ERROR POINTER TABLE

;; THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.  
;; THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN  
;; LOCATION SITE#B. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.  
;; NOTE1: IF SITE#B IS 0 THE ONLY PERTINENT DATA IS (SERRPC).  
;; NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;; \* EM ;; POINTS TO THE ERROR MESSAGE  
;; \* DH ;; POINTS TO THE DATA HEADER  
;; \* DT ;; POINTS TO THE DATA  
;; \* DF ;; POINTS TO THE DATA FORMAT

SERRTB:  
.EVEN

;; \* DF ;; DOES NOT APPLY IN THIS DIAGNOSTIC.

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381 001512  
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384 001512 000000  
385 001514 000000  
386 001516 000000  
387 001520 021330  
388 001522 021544  
389 001524 021620  
390 001526 021351  
391 001530 021544  
392 001532 021620  
393 001534 021330  
394 001536 021544  
395 001540 021636  
396 001542 021405  
397 001544 021576  
398 001546 021654  
399 001550 021421  
400 001552 021576  
401 001554 021654  
402 001556 021453  
403 001560 021544  
404 001562 021666  
405 001564 021501  
406 001566 021544  
407 001570 021704  
408 001572 021517  
409 001574 021576  
410 001576 021654  
411 002034  
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417 002034  
418 000024  
419 000024 000200  
420 000044  
421 000044 002034  
422 002034

.=2034  
.SBTTL APT PARAMETER BLOCK

\*\*\*\*\*  
; SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT  
\*\*\*\*\*  
; .SX= .; SAVE CURRENT LOCATION  
; .=24 .; SET POWER FAIL TO POINT TO START OF PROGRAM  
; 200 .; FOR APT START UP  
; .=44 .; POINT TO APT INDIRECT ADDRESS PNTR.  
; \$APTHDR .; POINT TO APT HEADER BLOCK  
; .= .SX .; RESET LOCATION COUNTER

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427 002034  
428 002034 000000  
429 002036 001316  
430 002040 000132  
431 002042 000137  
432 002044 000137  
433 002046 000052  
434

```

:*****
:SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-POP11 DIAGNOSTIC
:INTERFACE SPEC.

```

```

$APTHD:
$HIBTS: .WORD 0 ;; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
$MBAOR: .WORD $MAIL ;; ADDRESS OF APT MAILBOX (BITS 0-15)
$TSTM: .WORD 90. ;; RUN TIM OF LONGEST TEST
$PASTM: .WORD 95. ;; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
$UNITM: .WORD 95. ;; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
        .WORD $ETEND-$MAIL/2 ;; LENGTH MAILBOX-ETABLE(WORDS)

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002050 000000
002052 000000
002054 000000

002056 000000
002060 000000
002062 000000
002064 000000
002066 000000
002070 000000
002072 000000
002074 000000
002076 000000

002100 002100
002100 000001
002102 000001
002104 000001
002106 000001

002110 000001
002112 000001
002114 000001
002116 000001

002120 000001
002122 000001
002124 000001
002126 000001

002130 000001
002132 000001
002134 000001
002136 000001

002140 000001
002142 000001
002144 000001
002146 000001
    
```

;KMC11 CONTROL INDICATORS FOR CURRENT KMC11 UNDER TEST

```

-----
STAT1: 0
STAT2: 0
STAT3: 0
    
```

;KMC11 VECTOR AND REGISTER INDIRECT POINTERS

```

-----
KMRVEC: 0 ; POINTER TO KMC11 RECEIVER INTERRUPT VECTOR
KMRVLV: 0 ; POINTER TO KMC11 RECEIVER INTERRUPT SERVICE PS
KMTVEC: 0 ; POINTER TO KMC11 TRANSMITTER INTERRUPT VECTOR
KMTVLV: 0 ; POINTER TO KMC11 TRANSMITTER INTERRUPT SERVICE PS
KMCSR: 0 ; POINTER TO KMC11 CONTROL STATUS REGISTER
KMCSRH: 0 ; POINTER TO KMC11 CONTROL STATUS REGISTER HIGH BYTE.
KMCTL: 0 ; POINTER TO KMC11 CONTROL OUT REGISTER
KMP04: 0 ; POINTER TO KMC11 PORT REGISTER(SEL 4)
KMP06: 0 ; POINTER TO KMC11 PORT REGISTER(SEL 6)
    
```

;TEMP STORAGE

```

-----
;TEMP: 0
;.=.+40
    
```

;KMC11 STATUS TABLE AND ADDRESS ASSIGNMENTS

```

-----
.=2100
KM.MAP:
KMCRO0: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 00
KMS100: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 00
KMS200: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 00
KMS300: .BLKW 1 ; 3RD STATUS WORD

KMCRO1: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 01
KMS101: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 01
KMS201: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 01
KMS301: .BLKW 1 ; 3RD STATUS WORD

KMCRO2: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 02
KMS102: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 02
KMS202: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 02
KMS302: .BLKW 1 ; 3RD STATUS WORD

KMCRO3: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 03
KMS103: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 03
KMS203: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 03
KMS303: .BLKW 1 ; 3RD STATUS WORD

KMCRO4: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 04
KMS104: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 04
KMS204: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 04
KMS304: .BLKW 1 ; 3RD STATUS WORD
    
```





G03

DZKCD MACY11 27(1006) 12-MAY-77 18:42 PAGE 13  
DZKCD.P11 21-MAR-77 17:24 APT PARAMETER BLOCK  
547 002300 000000 KM.END: 000000

PAGE: 0032

```

548
549 ;KMC11 PASS COUNT AND ERROR COUNT TABLE
550 -----
551
552 CNT.MAP:
553 002302 000000 PACT00: 0 ;PASS COUNT FOR KMC11 NUMBER 00
554 002304 000000 ERCT00: 0 ;ERROR COUNT FOR KMC11 NUMBER 00
555
556 002306 000000 PACT01: 0 ;PASS COUNT FOR KMC11 NUMBER 01
557 002310 000000 ERCT01: 0 ;ERROR COUNT FOR KMC11 NUMBER 01
558
559 002312 000000 PACT02: 0 ;PASS COUNT FOR KMC11 NUMBER 02
560 002314 000000 ERCT02: 0 ;ERROR COUNT FOR KMC11 NUMBER 02
561
562 002316 000000 PACT03: 0 ;PASS COUNT FOR KMC11 NUMBER 03
563 002320 000000 ERCT03: 0 ;ERROR COUNT FOR KMC11 NUMBER 03
564
565 002322 000000 PACT04: 0 ;PASS COUNT FOR KMC11 NUMBER 04
566 002324 000000 ERCT04: 0 ;ERROR COUNT FOR KMC11 NUMBER 04
567
568 002326 000000 PACT05: 0 ;PASS COUNT FOR KMC11 NUMBER 05
569 002330 000000 ERCT05: 0 ;ERROR COUNT FOR KMC11 NUMBER 05
570
571 002332 000000 PACT06: 0 ;PASS COUNT FOR KMC11 NUMBER 06
572 002334 000000 ERCT06: 0 ;ERROR COUNT FOR KMC11 NUMBER 06
573
574 002336 000000 PACT07: 0 ;PASS COUNT FOR KMC11 NUMBER 07
575 002340 000000 ERCT07: 0 ;ERROR COUNT FOR KMC11 NUMBER 07
576
577 002342 000000 PACT10: 0 ;PASS COUNT FOR KMC11 NUMBER 10
578 002344 000000 ERCT10: 0 ;ERROR COUNT FOR KMC11 NUMBER 10
579
580 002346 000000 PACT11: 0 ;PASS COUNT FOR KMC11 NUMBER 11
581 002350 000000 ERCT11: 0 ;ERROR COUNT FOR KMC11 NUMBER 11
582
583 002352 000000 PACT12: 0 ;PASS COUNT FOR KMC11 NUMBER 12
584 002354 000000 ERCT12: 0 ;ERROR COUNT FOR KMC11 NUMBER 12
585
586 002356 000000 PACT13: 0 ;PASS COUNT FOR KMC11 NUMBER 13
587 002360 000000 ERCT13: 0 ;ERROR COUNT FOR KMC11 NUMBER 13
588
589 002362 000000 PACT14: 0 ;PASS COUNT FOR KMC11 NUMBER 14
590 002364 000000 ERCT14: 0 ;ERROR COUNT FOR KMC11 NUMBER 14
591
592 002366 000000 PACT15: 0 ;PASS COUNT FOR KMC11 NUMBER 15
593 002370 000000 ERCT15: 0 ;ERROR COUNT FOR KMC11 NUMBER 15
594
595 002372 000000 PACT16: 0 ;PASS COUNT FOR KMC11 NUMBER 16
596 002374 000000 ERCT16: 0 ;ERROR COUNT FOR KMC11 NUMBER 16
597
598 002376 000000 PACT17: 0 ;PASS COUNT FOR KMC11 NUMBER 17
599 002400 000000 ERCT17: 0 ;ERROR COUNT FOR KMC11 NUMBER 17
600

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FORMAT OF STATUS TABLE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00						
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	CSR					
I	C	O	N	T	R	O	L		R	E	G	I	S	T	E	R					
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I						
I	*	I	*	I	*	I	*	I	*	I	*	I	V	E	C	I	T	O	R	*	STAT1
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	*	B	M		A	D	D	*	I	*	L	I	N	E		*	*				STAT2
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	*	STAT3

DEFINITION OF FORMAT

- CSR: CONTAINS KMC11 CSR ADDRESS
- STAT1: BITS 00-08 IS KMC11 VECTOR ADDRESS  
 BIT14=1 ??? TURNAROUND CONNECTOR IS ON  
 BIT14=0 NO TURNAROUND CONNECTOR  
 BIT13=0 LINE UNIT IS AN M8201  
 BIT13=1 LINE UNIT IS AN M8202  
 BIT12=1 NO LINE UNIT  
 BITS 09-11 IS KMC11 BR PRIORITY LEVEL
- STAT2: LOW BYTE IS SWITCH PAC#1 (DOCMP LINE NUMBER)  
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)
- STAT3: BIT0=1 DO FREE RUNNING TESTS ON KMC  
 (MUST BE SET TO A ONE MANUALLY [PROGRAMS G AND H ONLY])

```

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662
663 002402 012737 000340 177776 .START: MOV #340,PS ;LOCK OUT INTERRUPTS
664 002410 012706 001200 MOV #STACK,SP ;SET UP STACK
665 002414 012737 007126 000024 MOV #SPWRDN,2#24 ;SET UP POWER FAIL VECTOR
666 002422 013737 001472 001476 MOV KMMUM,SAVNUM ;SAVE NUMBER OF DEVICES IN SYSTEM.
667 002430 005037 011416 CLR SWFLG ;CLEAR SOFT TYPEOUT FLAG
668 002434 105037 001203 CLR SERFLG ;CLEAR ERROR FLAG
669 002440 105037 001511 CLR QV.FLG ;ZERO QUICK VERIFY FLAG
670 002444 012737 002070 001502 MOV #KM.MAP-10,CREAM ;GET MAP POINTER.
671 002452 012737 002276 001504 MOV #CNT.MAP-4,MILK ;GET PASS COUNT MAP POINTER
672 002460 012737 100000 001500 MOV #BIT15,RUN ;POINT POINTER TO FIRST DEVICE.
673 002466 012700 002302 MOV #CNT.MAP,RO ;PASS COUNT POINTER TO RO
674 002472 005020 23$: CLR (RO)+ ;CLEAR TABLE
675 002474 022700 002402 CMP #CNT.MAP+100,RO ;DONE YET?
676 002500 001374 BNE 23$ ;KEEP GOING
677 002502 005037 001216 CLR $ERRPC ;CLEAR LAST ERROR POINTER
678 002506 012737 000001 001202 MOV #1,$STSTNM ;SET UP FOR TEST 1
679 002514 012737 002402 001206 MOV #.START,$LPADR ;SET UP FOR POWER FAIL BEFORE
680 ;TESTING STARTS
681 002522 132737 000001 001336 BITB #1,$ENV ;IS IT RUNNING UNDER APT?
682 002530 001404 BEQ 3$ ;IF NOT CHECK FOR TYPE OF SWITCH REGISTER.
683 002532 013737 001340 000176 MOV $SWREG,SWREG ;LOAD SOFTWARE SWITCH REG.
684 002540 000423 BR 6$+2 ;GO SET UP SOFTWARE SWITCH REG.
685 002542 013746 000006 3$: MOV 2#6,-(SP) ;SAVE CURRENT VECTORS
686 002546 013746 000004 MOV 2#4,-(SP)
687 002552 012737 002606 000004 MOV #6$,$2#4 ;SET UP FOR TIMEOUT
688 002560 012737 177570 1240 MOV #177570,SWR ;SET SWR TO HARD SWR ADDRESS
689 002566 012737 177570 001242 MOV #177570,DISPLAY ;SET DISPLAY TO HARD SWR ADDRESS
690 002574 022777 177777 176436 CMP #-1,$SWR ;REFERENCE HARDWARE SWITCH REGISTER
691 002602 001402 BEQ 6$+2 ;IF = -1 USE SOFT SWR ANYWAY
692 002604 000407 BR 7$ ;IF IT EXISTS AND NOT = -1 USE HARD SWR
693 002606 022626 6$: CMP (SP)+,(SP)+ ;ADJUST STACK
694 002610 012737 000176 001240 MOV #SWREG,SWR ;POINTER TO SOFT SWR
695 002616 012737 000174 001242 MOV #DISPREG,DISPLAY ;POINTER TO SOFT DISPLAY REG
696 002624 012637 000004 7$: MOV (SP)+,2#4 ;RESTORE VECTORS
697 002630 012637 000006 MOV (SP)+,2#6
698 002634 105737 001506 TSTB INIFLG ;HAS INITIALIZATION BEEN PERFORMED
699 002640 001036 BNE 20$ ;BR IF YES
700 002642 022737 004070 000042 CMP #SENDAD,2#42 ;IF ACT-11 AUTOMATIC MODE, DON'T TYPE ID
701 002650 001402 BEQ 20$
702 002652 104401 001000 TYPE ,MTITLE ;TYPE TITLE MESSAGE
703 002656 004737 011212 20$: JSR PC,CKSWR ;CHECK FOR SOFT SWR
704 002662 017737 176352 001446 MOV 2$SWR,STRTSW ;STORE STARTING SWITCHES
705 002670 005737 000042 TST 2#42 ;IS IT RUNNING IN AUTO MODE?
706 002674 001402 BEQ .+6 ;BR IF NO
707 002676 005037 001446 CLR STRTSW ;IF YES, CLEAR SWITCHES
708 002702 032737 000001 001446 BIT #SW00,STRTSW ;IF SW00=1, QUESTIONS ARE ASKED.
709 002710 001012 BNE 17$ ;BR IF SW00=1
710 002712 105737 001446 TSTB STRTSW ;BIT7=1??

```

PROGRAM INITIALIZATION AND START UP.

```

711 002716 100007          BPL      17$          ;BR IF SW07=0
712 002720 005737 001470  TST      KMACTV      ;ARE ANY DEVICES SELECTED?
713 002724 001027          BNE      16$          ;BR IF YES
714 002726 104401 010731  TYPE,    NOACT        ;NO DEVICES SELECTED.
715 002732 000000          HALT                    ;STOP THE SHOW
716 002734 000776          BR        .-2          ;DISQUALIFY CONTINUE SWITCH
717 002736 105737 001336  17$:    TSTB     $ENV      ;IS IT UNDER APT DUMP MODE?
718 002742 001405          BEQ      27$          ;YES, CHECK IF APT SIZED IT?
719 002744 132737 000001 001336  BITB     #1,$ENV      ;IS IT UNDER Q,V OR RUN MODE?
720 002752 001012          BNE      30$          ;YES, NEEDS ONLY APT SIZING.
721 002754 000406          BR        33$          ;NO, NEEDS REGULAR AUTO.SIZE.
722 002756 105737 001337  27$:    TSTB     $ENVM     ;IS IT SIZED BY APT?
723 002762 100406          BMI      30$          ;YES, NEEDS ONLY APT SIZING.
724 002764 042737 000001 001446  BIC      #SW00,STRTSW ;SIZE ONLY IN AUTO MODE.
725 002772 004737 012110  33$:    JSR      PC,AUTO.SIZE ;GO DO THE AUTO.SIZE.
726 002776 000402          BR        16$          ;GO PRINT THE MAP
727 003000 005737 013510  30$:    JSR      PC,APT.SIZE  ;GO DO THE APT SIZING.
728 003004 105737 001506  16$:    TSTB     INIFLG     ;FIRST TIME?
729 003010 001410          BEQ      21$          ;BR IF YES
730 003012 105737 001446  TSTB     STRTSW      ;IF USING SAME PARAMETERS DONT TYPE MAP
731 003016 100431          BMI      1$          ;
732 003020 032737 000006 001446  BIT      #BIT1!BIT2,STRTSW ;IS TEST NO. OR LOCK SELECTED
733 003026 001403          BEQ      24$          ;IF NO THEN TYPE STATUS
734 003030 000424          BR        1$          ;IF YES DO NOT TYPE STATUS
735 003032 105137 001506  21$:    COMB     INIFLG     ;SET FLAG
736 003036 104401 010077  24$:    TYPE     XHEAD      ;TYPE HEADER
737 003042 012704 002100  MOV      #KM.MAP,R4   ;SET POINTER
738 003046 010437 001276  5$:    MOV      R4,$TMP0    ;SET ADDRESS
739 003052 012437 001300  MOV      (R4)+,$TMP1  ;SET CSR
740 003056 001411          BEQ      1$          ;ALL DONE IF ZERO
741 003060 012437 001302  MOV      (R4)+,$TMP2  ;SET STAT1
742 003064 012437 001304  MOV      (R4)+,$TMP3  ;SET STAT2
743 003070 012437 001306  MOV      (R4)+,$TMP4  ;SET STAT3
744 003074 104416          CONVRT                    ;TYPE OUT STATUS MAP
745 003076 011060          XSTATQ                    ;
746 003100 000762          BR        5$          ;
747 003102 012700 002100  1$:    MOV      #KM.MAP,R0 ;R0 POINTS TO STATUS TABLE
748
749
750 ;*****
751 ;*AUTO SIZE TEST
752 ;*THIS TEST VERIFYS THAT THE KMC11S AND KMC11S ARE AT THE CORRECT FLOATING
753 ;*ADDRESSES FOR YOUR SYSTEM. IF THIS TEST FAILS, IT IS NOT A HARDWARE ERROR.
754 ;*CHECK THE ADDRESSES OF ALL FLOATING DEVICES (DJ,DM,DQ,DU,DUP,LK,DMC,DZ,KMC).
755 ;*IF THERE ARE NO OTHER FLOATING DEVICES BEFORE THE KMC11, THE FIRST
756 ;* KMC11 IS 760110. NO DEVICE SHOULD EVER BE AT
757 ;*ADDRESS 760000.
758 ;*****
759 003106 013746 000004          MOV      #4,-(SP)      ;SAVE LOC 4
760 003112 013746 000006          MOV      #6,-(SP)      ;SAVE LOC 6
761 003116 005037 000006          CLR      #6          ;CLEAR VEC+2
762 003122 005037 001302          CLR      $TMP2        ;CLEAR FLAG
763 003126 011037 002066  AUSTRT: MOV      (R0),KMC11 ;GET NEXT KMC CSR
764 003132 001510          BEQ      AHDONE        ;BR IF DONE
765 003134 012737 003240 000004  2$:    MOV      #NODEV,#4    ;SET UP FOR TIMEOUT
766 003142 012703 000010  3$:    MOV      #10,R3      ;R3 IS COUNT OF DEVICES BEFORE KMC

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PROGRAM INITIALIZATION AND START UP.

767	003146	012702	003342	4\$:	MOV	#DEVTAB,R2	;R2 IS DEVICE TABLE PONTER
768	003152	012701	160010		MOV	#160010,R1	;START WITH ADDRESS 160010
769	003156	005711		FLOAT:	TST	(R1)	;CHECK ADDRESS IN R1
770	003160	111204			MOVB	(R2),R4	;IF NO TIMEOUT, GET NEXT ADDRESS
771	003162	060401			ADD	R4,R1	;IN R1
772	003164	005201			INC	R1	
773	003166	040401			BIC	R4,R1	
774	003170	005703			TST	R3	;ANY MORE DEVICES TO CHECK FOR?
775	003172	001371			BNE	FLOAT	;BR IF YES
776	003174	012737	003244 000004		MOV	#ERR,2#4	;OK ONLY KMC'S ARE LEFT, SET UP FOR TIMEOUT
777	003202	005711		FY:	TST	(R1)	;CHECK KMC ADDRESS
778	003204	020137	002066		CMP	R1,KMCSR	;DOES IT MATCH
779	003210	001403			BEQ	OK	;BR IF YES
780	003212	062701	000010		ADD	#10,R1	;GET NEXT KMC ADDRESS
781	003216	000771			BR	FY	;DO IT AGAIN
782	003220	062700	000010	OK:	ADD	#10,R0	;SKIP TO NEXT KMC CSR
783	003224	062701	000010		ADD	#10,R1	;GET NEXT KMC ADDRESS
784	003230	011037	002066		MOV	(R0),KMCSR	;GET NEXT KMC CSR
785	003234	001447			BEQ	AUDONE	;BRANCH IF ALL DONE.
786	003236	000761			BR	FY	;DO IT AGAIN.
787	003240	122243		NODEV:	CMPB	(R2)+,-(R3)	;ON TIMEOUT, INC R2, DEC R3
788	003242	000002			RTI		;SLPADR
789	003244	005737	001302	ERR:	TST	\$TMP2	;CHECK FLAG IF = 0 TYPE HEADER
790	003250	001014			BNE	IS	;SKIP HEADER
791	003252	104401			TYPE		;TYPEOUT HEADER MESSAGE
792	003254	010762			CONERR		;CONFIGURATION ERROR!!!!
793	003256	012737	003244 001460		MOV	#ERR,SAVPC	;SAVE PC FOR TYPEOUT
794	003264	104417			CNVRT		;TYPE OUT ERROR PC
795	003266	003322			ERRPC		
796	003270	104401			TYPE		;TYPE REST OF HEADER
797	003272	011027			CNERR		
798	003274	012737	177777 001302		MOV	#-1,\$TMP2	;SET FLAG SO IT ONLY GETS TYPED ONCE
799	003302	010137	001264	IS:	MOV	R1,\$REG1	;SAVE R1 FOR TYPEOUT
800	003306	104416			CONVRT		
801	003310	003330			CONTAB		;TYPE CSR VALUES
802	003312	104401		3\$:	TYPE		
803	003314	011050			KMCM		
804	003316	022626		4\$:	CMP	(SP)+,(SP)+	;ADJUST STACK
805	003320	000737			BR	OK	;BR TO GET OUT
806	003322	000001		ERRPC:	1		
807	003324	006	002		.BYTE	6,2	
808	003326	001460			SAVPC		
809	003330	000002		CONTAB:	2		
810	003332	006	004		.BYTE	6,4	
811	003334	001261			\$REG1		
812	003336	006	002		.BYTE	6,2	
813	003340	002066			KMCSR		
814	003342	007		DEVTAB:	.BYTE	7	;DJ
815	003343	017			.BYTE	17	;DH
816	003344	007			.BYTE	7	;DQ
817	003345	007			.BYTE	7	;DU
818	003346	007			.BYTE	7	;DUP
819	003347	007			.BYTE	7	;LK
820	003350	007			.BYTE	7	;DMC
821	003351	007			.BYTE	7	;DZ
822	003352	007			.BYTE	7	;KMC



N03

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PROGRAM INITIALIZATION AND START UP.

879	003634	012737	011460	001206	3\$:	MOV	#CYCLE,SLPADR	;START AT "CYCLE" FIND WHICH DEVICE TO TEST
880	003642	032737	000002	001446	4\$:	BIT	#SW01,STRTSW	;IS TEST NO. SELECTED?
881	003650	001002				BNE	\$S	;OR IF YES
882	003652	104401	007642			TYPE	MR	;TYPE R
883	003656	000177	175324		5\$:	JMP	\$SLPADR	;START TESTING



:END OF PASS  
:TYPE NAME OF TEST  
:UPDATE PASS COUNT  
:CHECK FOR EXIT TO ACT-11  
:RESTART TEST

.SBTTL END OF PASS ROUTINE

\*\*\*\*\*  
:INCREMENT THE PASS NUMBER (\$PASS)  
:IF THERES A MONITOR GO TO IT  
:IF THERE ISN'T JUMP TO CYCLE

SEOP:

894					
895					
896					
897					
898					
899					
899	003662	000005			
900	003664	005237	001324		
901	003670	105037	001203		
902	003674	104401	007620		
903	003700	104401	007745		
904	003704	104417	004104		
905	003710	104401	007753		
906	003714	104417	004112		
907	003720	104401	007761		
908	003724	104417	004120		
909	003730	104401	007772		
910	003734	104417	004126		
911	003740	013700	001504		
912	003744	013720	001324		
913	003750	013720	001212		
914	003754	013777	002060	176074	
915	003762	005077	176072		
916	003766	013777	002064	176066	
917	003774	005077	176064		
918	004000	005337	001476		
919	004004	001035			
920	004006	112737	000377	001511	
921	004014	013737	001472	001476	
922	004022	005037	001216		
923	004026	005037	001310		
924	004032	005237	001324		
925	004036	042737	100000	001324	
926	004044	005327			
927	004046	000001			
928	004050	003013			
929	004052	012737			
930	004054	000001			
931	004056	004046			
932	004060	013700	000042		
933	004064	001405			
934	004066	000005			
935	004070	004710			
936	004072	000240			
937	004074	000240			
938	004076	000240			
939	004100	000137			

RESET				INCREMENT THE PASS COUNT
INC	\$PASS			CLEAR ERROR FLAG
CLRB	\$ERFLG			TYPE END PASS.
TYPE	,MEPASS			TYPE "CSR"
TYPE	,MCSR			SHOW IT.
CMVRT	,XCSR			TYPE VECTOR.
TYPE	,MVECX			SHOW IT.
CMVRT	,XVEC			TYPE " PASSES "
TYPE	,MPASSX			SHOW IT.
CMVRT	,XPASS			TYPE " ERRORS "
TYPE	,MERRX			SHOW IT.
CMVRT	,XERR			SET POINTER TO PASSCNT.
MOV	\$ILK,RO			SAVE THE PASS COUNT.
MOV	\$PASS,(RO)+			SAVE ERROR COUNT
MOV	\$ERTTL,(RO)+			RESTORE THE RECEIVER INTERRUPT VECTOR.
MOV	\$KRLVL,@KMRVEC			RESTORE RECEIVER LEVEL
CLR	@KRLVL			RESTORE THE TRANSMIT INTERRUPT VECTOR.
MOV	\$KTLVL,@KMTVEC			RESTORE TRANSMITTER LEVEL
CLR	@KTLVL			ALL DEVICE TESTED?
DEC	\$AVNUM			BRANCH IF NO.
BNE	\$DOAGN			SET QUICK VERIFY FLAG.
MOV	\$377,@V.FLG			RESTORE DEVICE COUNT.
MOV	\$KAVNUM,\$AVNUM			CLEAR LAST ERROR PC
CLR	\$ERRPC			ZERO THE NUMBER OF ITERATIONS
CLR	\$TIMES			INCREMENT THE PASS NUMBER
INC	\$PASS			DON'T ALLOW A NEG. NUMBER
BIC	\$100000,\$PASS			LOOP?
DEC	(PC)+			
SEOPCT:	.WORD	1		:: YES
BGT	\$DOAGN			:: RESTORE COUNTER
MOV	(PC)+,@(PC)+			
SENDCT:	.WORD	1		
SEOPCT				
\$GET42:	MOV	@#42,RO		:: GET MONITOR ADDRESS
BFG	\$DOAGN			:: BRANCH IF NO MONITOR
RESET				:: CLEAR THE WORLD
SENDAD:	J	PC,(RO)		:: GO TO MONITOR
NOP				:: SAVE ROOM
NOP				:: FOR
NOP				:: ACT11
\$DOAGN:				
JMP	@(PC)+			:: RETURN

940	004102	011460	
941	004104	000001	
942	004106	006	002
943	004110	002066	
944	004112	000001	
945	004114	004	002
946	004116	002056	
947	004120	000001	
948	004122	006	002
949	004124	001324	
950	004126	000001	
951	004128	006	002
952	004132	001212	

```

$RTNAD: .WORD   CYCLE
XCSR:   1
        .BYTE   6,2
        KMCSR
XVEC:   1
        .BYTE   4,2
        KMRVEC
XPASS:  1
        .BYTE   6,2
        $PASS
XERR:   1
        .BYTE   6,2
        $ERTTL

```

; SCOPE LOOP AND INTERATION HANDLER  
-----

.SBTTL SCOPE HANDLER ROUTINE

953			
954			
955			
956			
957			
958			
959			
960			
961			
962			
963			
964			
965			
966			
967			
968			
969	004134		
970	004134	005037	001216
971	004140	023716	013734
972	004144	001413	
973	004146	000406	
974	004150	105777	175070
975	004154	100067	
976	004156	017766	175064 177776
977	004164	032777	040000 175046
978	004172	001060	
979			
980	004174	000416	
981			
982	004176	013746	000004
983	004202	012737	004222 000004
984	004210	005737	177060
985	004214	012637	000004
986	004220	000436	
987	004222	022626	
988	004224	012637	000004
989	004230	000441	
990	004232		
991	004232	105737	001203
992	004236	001404	
993	004240	105037	001203
994	004244	005037	001310
995	004250	032777	004000 174762

```

; *****
; THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
; AND LOAD THE TEST NUMBER($TSTNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
; AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
; THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
; SW14=1      LOOP ON TEST
; SW11=1      INHIBIT ITERATIONS
; CALL
; *          SCOPE          ;;SCOPE=IOT

$SCOPE:  CLR      $ERRPC          ; CLEAR LAST ERROR PC
          CMP      TST1+2,(SP)    ; IS THIS TEST #1 ?
          BEQ      $XTSTR        ; IF SO DON'T LOOP.
TTST:    BR       'S
          TSTB     @STKS          ; KEYBOARD DONE ?
          BPL      $OVER         ; IF NO DONT WAIT.
          MOV      @STKB,-2(SP)
1$:      BIT      @BIT14,@SWR    ;; LOOP ON PRESENT TEST?
          BNE      $OVER         ;; YES IF SW14=1
; *****START OF CODE FOR THE XOR TESTER*****
$XTSTR:  BR       6$
          MOV      @ERRVEC,-(SP)  ; IF RUNNING ON THE "XOR" TESTER CHANGE
          MOV      @ERRVEC       ; THIS INSTRUCTION TO A "NOP" (NOP=240)
          TST      @177060       ; SAVE THE CONTENTS OF THE ERROR VECTOR
          MOV      (SP)+,@ERRVEC  ; SET FOR TIMEOUT
          BR       $SVLAD        ; TIME OUT ON XOR?
          CMP      (SP)+,(SP)+    ; RESTORE THE ERROR VECTOR
          MOV      (SP)+,@ERRVEC  ; GO TO THE NEXT TEST
          BR       $OVER         ; CLEAR THE STACK AFTER A TIME OUT
          BR       $OVER         ; RESTORE THE ERROR VECTOR
          BR       $OVER         ; LOOP ON THE PRESENT TEST
6$:      ; *****END OF CODE FOR THE XOR TESTER*****
2$:      TSTB     $ERFLG        ; HAS AN ERROR OCCURRED?
          BEQ      'S          ; BR IF NO
          CLRB    $ERFLG       ; ZERO THE ERROR FLAG
          CLR     $TIMES        ; CLEAR THE NUMBER OF ITERATIONS TO MAKE
          BIT     @BIT11,@SWR   ; INHIBIT ITERATIONS?

```

SCOPE HANDLER ROUTINE

```

996 004256 001011          BNE      IS
997 004260 005737 001324    TST      $PASS          ;; BR IF YES
998 004264 001406          BEQ      IS              ;; IF FIRST PASS OF PROGRAM
999 004266 005237 001204    INC      $ICNT          ;; INHIBIT ITERATIONS
1000 004272 023737 001310 001204  CMP      $TIMES,$ICNT  ;; INCREMENT ITERATION COUNT
1001 004300 002015          BGE      $OVER          ;; CHECK THE NUMBER OF ITERATIONS MADE
1002 004302 012737 000001 001204 1S:  MOV     $I, $ICNT      ;; BR IF MORE ITERATION REQUIRED
1003 004310 013737 004362 001310  MOV     $SMXCNT,$TIMES ;; REINITIALIZE THE ITERATION COUNTER
1004 004316 105237 001202 001310  $SVLAD: INCB   $STNM     ;; SET NUMBER OF ITERATIONS TO DO
1005 004322 113737 001202 001322  MOV     $STNM,$STESTN  ;; COUNT TEST NUMBERS
1006 004330 011637 001206          MOV     (SP), $LPADR   ;; SET TEST NUMBER IN APT MAILBOX
1007 004334 013777 001202 174700 $OVER:  MOV     $STNM,$DISPLAY ;; SAVE SCOPE LOOP ADDRESS
1008 004342 013716 001206          MOV     $LPADR,(SP)   ;; DISPLAY TEST NUMBER
1009 004346 005037 001444          CLR     LOCK          ;; FUDGE RETURN ADDRESS
1010 004352 013701 002066          MOV     KMCSR,R1     ;; RESET LOCK ON DATA.
1011 004356 000002          RTI                    ;; R1 CONTAINS BASE KMC ADDRESS.
1012 004360 000406          BRW:   .WORD    406
1013 004362 000020          $SMXCNT: 20          ;;MAX. NUMBER OF ITERATIONS
1014
1015          ;;CHECK FOR FREEZE ON CURRENT DATA
1016          -----
1017
1018 004364 004737 011212 174642 .SCOPI: JSR     PC,CKSWR          ;;CHECK FOR SOFT SWR
1019 004370 032777 001000 174642  BIT     #SW09,$SWR     ;;IS SW09=1(SET)?
1020 004376 001405          BEQ     IS              ;;BR IF NOT SET.
1021 004400 005737 001444          TST     LOCK
1022 004404 001402          BEQ     IS
1023 004406 013716 001444          MOV     LOCK,(SP)    ;;GOTO THE ADDRESS IN LOCK.
1024 004412 000002 1S:      RTI              ;;GO BACK.
1025
1026          ;;TELETYPE OUTPUT ROUTINE
1027          -----
1028
1029          .SBTTL  TYPE ROUTINE
1030
1031          ;*****
1032          ;ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
1033          ;THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
1034          ;*NOTE1:          $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
1035          ;*NOTE2:          $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
1036          ;*NOTE3:          $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
1037          ;*
1038          ;CALL:
1039          ;1) USING A TRAP INSTRUCTION
1040          ;*      TYPE      ,MESADR          ;;MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
1041          ;*OR
1042          ;*      TYPE
1043          ;*      MESADR
1044          ;*
1045
1046 004414 105737 001257  STYPE:  TSTB   $TPFLG          ;; IS THERE A TERMINAL?
1047 004420 100002          BPL     IS              ;; BR IF YES
1048 004422 000000          HALT                    ;; HALT HERE IF NO TERMINAL
1049 004424 000430          BR     3$              ;; LEAVE
1050 004426 010046 1S:      MOV     R0,-(SP)      ;; SAVE R0
1051 004430 017600 000002  MOV     @2(SP),R0      ;; GET ADDRESS OF ASCIZ STRING

```



APT COMMUNICATIONS ROUTINE

.SBTTL APT COMMUNICATIONS ROUTINE

```

1108
1109
1110
1111 004676 112737 000001 005142 $ATY1: MOV  #1,$FFLG ;; TO REPORT FATAL ERROR
1112 004704 112737 000001 005140 $ATY3: MOV  #1,$MFLG ;; TO TYPE A MESSAGE
1113 004712 000403
1114 004714 112737 000001 005142 $ATY4: MOV  #1,$FFLG ;; TO ONLY REPORT FATAL ERROR
1115 004722 $ATYC:
1116 004722 010046 MOV  R0,-(SP) ;; PUSH R0 ON STACK
1117 004724 010146 MOV  R1,-(SP) ;; PUSH R1 ON STACK
1118 004726 105737 005140 TSTB $MFLG ;; SHOULD TYPE A MESSAGE?
1119 004732 001450 BEQ  $S ;; IF NOT: BR
1120 004734 122737 000001 001336 CMPB  $APTENV,$ENV ;; OPERATING UNDER APT?
1121 004742 001031 BNE  $S ;; IF NOT: BR
1122 004744 132737 000100 001337 BITB  $APTPOOL,$ENVM ;; SHOULD SPOOL MESSAGES?
1123 004752 001425 BEQ  $S ;; IF NOT: BR
1124 004754 017600 000004 MOV  #24(SP),R0 ;; GET MESSAGE ADDR.
1125 004760 062766 000002 000004 ADD  #2,4(SP) ;; BUMP RETURN ADDR.
1126 004766 005737 001316 1$: TST  $MSGTYPE ;; SEE IF DONE W/ LAST XMISSION?
1127 004772 001375 BNE  $S ;; IF NOT: WAIT
1128 004774 010037 001332 MOV  R0,$MSGAD ;; PUT ADDR IN MAILBOX
1129 005000 105720 2$: TSTB (R0)+ ;; FIND END OF MESSAGE
1130 005002 001376 BNE  $S
1131 005004 163700 001332 SUB  $MSGAD,R0 ;; SUB START OF MESSAGE
1132 005010 006200 ASR  R0 ;; GET MESSAGE LGTH IN WORDS
1133 005012 010037 001334 MOV  R0,$MSGLG ;; PUT LENGTH IN MAILBOX
1134 005016 012737 000004 001316 MOV  #4,$MSGTYPE ;; TELL APT TO TAKE MSG.
1135 005024 000413 BR   $S
1136 005026 017637 000004 005052 3$: MOV  #24(SP),#4 ;; PUT MSG ADDR IN JSR LINKAGE
1137 005034 062766 000002 000034 ADD  #2,4(SP) ;; BUMP RETURN ADDRESS
1138 005042 013746 177776 MOV  177776,-(SP) ;; PUSH 177776 ON STACK
1139 005046 004737 004414 JSR  PC,$TYPE ;; CALL TYPE MACRO
1140 005052 000000 4$: .WORD 0
1141 005054 5$:
1142 005054 105737 005142 10$: TSTB $FFLG ;; SHOULD REPORT FATAL ERROR?
1143 005060 001416 BEQ  $S ;; IF NOT: BR
1144 005062 005737 001336 TST  $ENV ;; RUNNING UNDER APT?
1145 005066 001413 BEQ  $S ;; IF NOT: BR
1146 005070 005737 001316 11$: TST  $MSGTYPE ;; FINISHED LAST MESSAGE?
1147 005074 001375 BNE  $S ;; IF NOT: WAIT
1148 005076 017637 000004 001320 MOV  #24(SP),$FATAL ;; GET ERROR #
1149 005104 062766 000002 000004 ADD  #2,4(SP) ;; BUMP RETURN ADDR.
1150 005112 005237 001316 INC  $MSGTYPE ;; TELL APT TO TAKE ERROR
1151 005116 105037 005142 12$: CLRB $FFLG ;; CLEAR FATAL FLAG
1152 005122 105037 005141 CLRB $LFLG ;; CLEAR LOG FLAG
1153 005126 105037 005140 CLRB $MFLG ;; CLEAR MESSAGE FLAG
1154 005132 012601 MOV  (SP)+,R1 ;; POP STACK INTO R1
1155 005134 012600 MOV  (SP)+,R0 ;; POP STACK INTO R0
1156 005136 000207 RTS  PC ;; RETURN
1157 005140 000 $MFLG: .BYTE 0 ;; MESSG. FLAG
1158 005141 000 $LFLG: .BYTE 0 ;; LOG FLAG
1159 005142 000 $FFLG: .BYTE 0 ;; FATAL FLAG
1160 005144 .EVEN
1161 000200 APTSIZE=200
1162 000001 APTENV=001
1163 000100 APTPOOL=100

```

APTCSUP=040

.SBTTL TTY INPUT ROUTINE

\*\*\*\*\*

.ENABL LSB

.DSABL LSB

\*\*\*\*\*

\*THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY

\*CALL:

\* RDCHR ;: INPUT A SINGLE CHARACTER FROM THE TTY  
\* RETURN HERE ;: CHARACTER IS ON THE STACK  
\* ;: WITH PARITY BIT STRIPPED OFF

1164 000040  
1165  
1166  
1167  
1168  
1169  
1170  
1171  
1172  
1173  
1174  
1175  
1176  
1177  
1178  
1179  
1180  
1181  
1182  
1183 005144 011646  
1184 005146 016666 000004 000002  
1185 005154 105777 174064  
1186 005160 100375  
1187 005162 117766 174060 000004  
1188 005170 042766 177600 000004  
1189 005176 026627 000004 000023  
1190 005204 001013  
1191 005206 105777 174032 25:  
1192 005212 100375  
1193 005214 117746 174026  
1194 005220 042716 177600  
1195 005224 022627 000021  
1196 005230 001366  
1197 005232 000750  
1198 005234 026627 000004 000140 35:  
1199 005242 002407  
1200 005244 026627 000004 000175  
1201 005252 003003  
1202 005254 042766 000040 000004  
1203 005262 000002 45:  
1204  
1205  
1206  
1207  
1208  
1209  
1210  
1211 005264 010346  
1212 005266 005046  
1213 005270 012703 005520  
1214 005274 022703 005527  
1215 005300 101456  
1216 005302 104402  
1217 005304 112613  
1218 005306 122713 000177  
1219 005312 001022

\$RDCHR: MOV (SP), -(SP) ;: PUSH DOWN THE PC  
MOV 4(SP), 2(SP) ;: SAVE THE PS  
15: TSTB 2\$TKS ;: WAIT FOR  
BPL 1\$ ;: A CHARACTER  
MOVB 2\$TKB, 4(SP) ;: READ THE TTY  
BIC #1C(177), 4(SP) ;: GET RID OF JUNK IF ANY  
CMP 4(SP), #23 ;: IS IT A CONTROL-S?  
BNE 3\$ ;: BRANCH IF NO  
25: TSTB 2\$TKS ;: WAIT FOR A CHARACTER  
BPL 2\$ ;: LOOP UNTIL ITS THERE  
MOVB 2\$TKB, -(SP) ;: GET CHARACTER  
BIC #1C(177), (SP) ;: MAKE IT 7-BIT ASCII  
CMP (SP)+, #21 ;: IS IT A CONTROL-Q?  
BNE 2\$ ;: IF NOT DISCARD IT  
BR 1\$ ;: YES, RESUME  
35: CMP 4(SP), #140 ;: IS IT UPPER CASE?  
BLT 4\$ ;: BRANCH IF YES  
CMP 4(SP), #175 ;: IS IT A SPECIAL CHAR?  
BGT 4\$ ;: BRANCH IF YES  
BIC #40, 4(SP) ;: MAKE IT UPPER CASE  
45: RTI ;: GO BACK TO USER

\*\*\*\*\*

\*THIS ROUTINE WILL INPUT A STRING FROM THE TTY

\*CALL:

\* RDLIN ;: INPUT A STRING FROM THE TTY  
\* RETURN HERE ;: ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK  
\* ;: TERMINATOR WILL BE A BYTE OF ALL 0'S

\$RDLIN: MOV R3, -(SP) ;: SAVE R3  
CLR -(SP) ;: CLEAR THE RUBOUT KEY  
15: MOV #1\$TTYIN, R3 ;: GET ADDRESS  
25: CMP #1\$TTYIN+7, R3 ;: BUFFER FULL?  
BLOS 4\$ ;: BR IF YES  
RDCHR ;: GO READ ONE CHARACTER FROM THE TTY  
MOVB (SP)+, (R3) ;: GET CHARACTER  
105: CMPB #177, (R3) ;: IS IT A RUBOUT  
BNE 5\$ ;: BR IF NO

```

1220 005314 005716          TST      (SP)          ;; IS THIS THE FIRST RUBOUT?
1221 005316 001007          BNE     6$            ;; BR IF NO
1222 005320 112737 000134 005516  MOV     #' \, 9$      ;; TYPE A BACK SLASH
1223 005326 104401 005516          TYPE    9$
1224 005332 012716 177777          MOV     1-1, (SP)    ;; SET THE RUBOUT KEY
1225 005336 005303          DEC     R3           ;; BACKUP BY ONE
1226 005340 020327 005520          CMP     R3, #STTYIN ;; STACK EMPTY?
1227 005344 103434          BLO    4$           ;; BR IF YES
1228 005346 111337 005516          MOV     (R3), 9$     ;; SETUP TO TYPEOUT THE DELETED CHAR.
1229 005352 104401 005516          TYPE    9$          ;; GO TYPE
1230 005356 000746          BR     2$           ;; GO READ ANOTHER CHAR.
1231 005360 005716          TST     (SP)         ;; RUBOUT KEY SET?
1232 005362 001406          BEQ    7$           ;; BR IF NO
1233 005364 112737 000134 005516  MOV     #' \, 9$      ;; TYPE A BACK SLASH
1234 005372 104401 005516          TYPE    9$
1235 005376 005016          CLR     (SP)         ;; CLEAR THE RUBOUT KEY
1236 005400 122713 000025          CMP     #25, (R3)    ;; IS CHARACTER A CTRL U?
1237 005404 001003          BNE    8$           ;; BR IF NO
1238 005406 104401 005527          TYPE    $CNTLU      ;; TYPE A CONTROL "U"
1239 005412 000726          BR     1$           ;; GO START OVER
1240 005414 122713 000022          CMP     #22, (R3)    ;; IS CHARACTER A "TR"?
1241 005420 001011          BNE    3$           ;; BRANCH IF NO
1242 005422 105013          CLRB   (R3)         ;; CLEAR THE CHARACTER
1243 005424 104401 001313          TYPE    , $SCRLF    ;; TYPE A "CR" & "LF"
1244 005430 104401 005520          TYPE    $STTYIN     ;; TYPE THE INPUT STRING
1245 005434 000717          BR     2$           ;; GO PICKUP ANOTHER CHARACTER
1246 005436 104401 001312          TYPE    $QUES       ;; TYPE A '?'
1247 005442 000712          BR     1$           ;; CLEAR THE BUFFER AND LOOP
1248 005444 111337 005516          MOV     (R3), 9$     ;; ECHO THE CHARACTER
1249 005450 104401 005516          TYPE    9$
1250 005454 122723 000015          CMP     #15, (R3)+   ;; CHECK FOR RETURN
1251 005460 001305          BNE    2$           ;; LOOP IF NOT RETURN
1252 005462 105063 177777          CLRB   -1(R3)       ;; CLEAR RETURN (THE 15)
1253 005466 104401 001314          TYPE    $LF         ;; TYPE A LINE FEED
1254 005472 005726          TST     (SP)+       ;; CLEAN RUBOUT KEY FROM THE STACK
1255 005474 012603          MOV     (SP)+, R3    ;; RESTORE R3
1256 005476 011646          MOV     (SP), -(SP) ;; ADJUST THE STACK AND PUT ADDRESS OF THE
1257 005500 016666 000004 000002  MOV     4(SP), 2(SP) ;; FIRST ASCII CHARACTER ON IT
1258 005506 012766 005520 000004  MOV     #STTYIN, 4(SP)
1259 005514 000002          RTI
1260 005516 000          9$: .BYTE 0          ;; RETURN
1261 005517 000          .BYTE 0          ;; STORAGE FOR ASCII CHAR. TO TYPE
1262 005520 000007  $STTYIN: .BLKB 7    ;; TERMINATOR
1263 005527 136 006525 000012 $CNTLU: .ASCIZ /?U/<15><12> ;; RESERVE 7 BYTES FOR TTY INPUT
1264 005534 043536 005015 000 $CNTLG: .ASCIZ /?G/<15><12> ;; CONTROL "U"
1265 005541 015 051412 051127 $MSWR: .ASCIZ <15><12>/SWR = / ;; CONTROL "G"
1266 005546 036440 000040
1267 005552 020040 042516 020127 $MNEW: .ASCIZ / NEW = /
1268 005560 020075 000
1269 005564
1270 .EVEN
1271 .SBTTL READ AN OCTAL NUMBER FROM THE TTY
1272
1273 ;*****
1274 ;THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
1275 ;CHANGE IT TO BINARY.
1276 ;THE INPUT CHARACTERS WILL BE CHECKED TO INSURED THEY ARE LEGAL

```

```

1276
1277
1278
1279
1280
1281
1282
1283
1284 005564 011646
1285 005566 016666 000004 000002
1286 005574 010046
1287 005576 010146
1288 005600 010246
1289 005602 104403
1290 005604 012600
1291 005606 010037 005712
1292 005612 005001
1293 005614 005002
1294 005616 112046
1295 005620 001420
1296 005622 122716 000060
1297 005626 003026
1298 005630 122716 000067
1299 005634 002423
1300 005636 006301
1301 005640 006102
1302 005642 006301
1303 005644 006102
1304 005646 006301
1305 005650 006102
1306 005652 042716 177770
1307 005656 062601
1308 005660 000756
1309 005662 005726
1310 005664 010166 000012
1311 005670 010237 005722
1312 005674 012602
1313 005676 012601
1314 005700 012600
1315 005702 000002
1316 005704 005726
1317 005706 105010
1318 005710 104401
1319 005712 000000
1320 005714 104401 001312
1321 005720 000730
1322 005722 000000
1323
1324
1325
1326
1327 005724 010546
1328 005726 016605 000002
1329 005732 012537 005770
1330 005736 012537 006050
1331 005742 012537 006052

```

```

: *OCTAL DIGITS. IF AN ILLEGAL CHARACTER IS READ A "?" WILL BE TYPED
: *FOLLOWED BY A CARRIAGE RETURN-LINE FEED. THE COMPLETE NUMBER MUST
: *THEN BE RETYPED. THE INPUT IS TERMINATED BY TYPING A CARRIAGE RETURN.
: *CALL:
: *   RDOCT
: *   RETURN HERE
: *
: * READ AN OCTAL NUMBER
: * LOW ORDER BITS ARE ON TOP OF THE STACK
: * HIGH ORDER BITS ARE IN $HI OCT

```

```

$RDOCT: MOV (SP), -(SP) ; PROVIDE SPACE FOR THE
MOV 4(SP), 2(SP) ; INPUT NUMBER
MOV R0, -(SP) ; PUSH R0 ON STACK
MOV R1, -(SP) ; PUSH R1 ON STACK
MOV R2, -(SP) ; PUSH R2 ON STACK
1$: ROLIM ; READ AN ASCII LINE
MOV (SP)+, R0 ; GET ADDRESS OF 1ST CHARACTER
MOV R0, 5$ ; AND SAVE IT
CLR R1 ; CLEAR DATA WORD
CLR R2
2$: MOVB (R0)+, -(SP) ; PICKUP THIS CHARACTER
BEQ 3$ ; IF ZERO GET OUT
CMPB #'0, (SP) ; MAKE SURE THIS CHARACTER
BGT 4$ ; IS AN OCTAL DIGIT
CMPB #'7, (SP)
BLT 4$
ASL R1 ; *2
ROL R2
ASL R1 ; *4
ROL R2
ASL R1 ; *8
ROL R2
BIC #'C7, (SP) ; STRIP THE ASCII JUNK
ADD (SP)+, R1 ; ADD IN THIS DIGIT
BR 2$ ; LOOP
3$: TST (SP)+ ; CLEAN TERMINATOR FROM STACK
MOV R1, 12(SP) ; SAVE THE RESULT
MOV R2, $HI OCT
MOV (SP)+, R2 ; POP STACK INTO R2
MOV (SP)+, R1 ; POP STACK INTO R1
MOV (SP)+, R0 ; POP STACK INTO R0
RTI ; RETURN
4$: TST (SP)+ ; CLEAN PARTIAL FROM STACK
CLRB (R0) ; SET A TERMINATOR
TYPE ; TYPE UP THRU THE BAD CHAR.
5$: .WORD 0 ; "?" "CR" & "LF"
TYPE $QUES ; TRY AGAIN
BR 1$
$HI OCT: .WORD 0 ; HIGH ORDER BITS GO HERE

```

INPUT OCTAL NUMBER ROUTINE

```

$INPUT: MOV R5, -(SP) ; SAVE REGISTER R5.
MOV 2(SP), R5 ; GET FIRST PARAMETER ADDRESS.
MOV (R5)+, WHAT ; GET MESSAGE ADDRESS.
MOV (R5)+, LOLIM ; GET LOW LIMIT FOR THE #
MOV (R5)+, HILIM ; GET HIGH LIMIT FOR THE #.

```



```

1332 005746 012537 006054      MOV      (R5)+,WHERE      ; GET ADDRESS OF INBUFFER
1333 005752 112537 006056      MOVB    (R5)+,LOBITS     ; GET LOWMASK BITS.
1334 005756 112537 006057      MOVB    (R5)+,ADRCNT     ; GET # OF #'S TO BE GENERATED.
1335 005762 010566 000002      MOV     RS,2(SP)        ; SAVE THE RETURN ADDRESS.
1336 005766 104401                INLPI:  TYPE             ; TYPE THE MESSAGE.
1337 005770 000000      WHAT:   .WORD          0
1338 005772 104404                RDOCT
1339 005774 021637 006052      CMP     (SP),HILIM      ; READ OCTAL # FROM KEYBOARD.
1340 006000 003003                BGT     2$              ; IS IT IN HIGH LIMIT?
1341 006002 021637 006050      CMP     (SP),LOLIM      ; BRANCH IF NO.
1342 006006 002005                BGE     3$              ; IS IT MORE THAN LOW LIMIT.
1343 006010 104401 001312      2$:     TYPE             ; BRANCH IF YES.
1344 006014 104401 001313      TYPE    ,SQUES          ; TYPE " ? "
1345 006020 000762                BR      INLPI           ; TYPE <CR>,<LF>
1346 006022 013705 006054      3$:     MOV     WHERE,R5   ; GET BUFFER ADDRESS.
1347 006026 011625 4$:     MOV     (SP),(R5)+     ; SAVE THE # IN RIGHT PLACE.
1348 006030 062716 000002      ADD     #2,(SP)         ; NEXT SEQUENTIAL NUMBER.
1349 006034 105337 006057      DECB   ADRCNT          ; COUNT BY 1.
1350 006040 001372                BNE     4$              ; BRANCH IF NOT DONE.
1351 006042 005726                TST     (SP)+           ; POP THE STACK POINTER.
1352 006044 012605                MOV     (SP)+,R5       ; POP THE REG.5
1353 006046 000002      RTI
1354 006050 000000      LOLIM:  .WORD          0
1355 006052 000000      HILIM:  .WORD          0
1356 006054 000000      WHERE:  .WORD          0
1357 006056 000          LOBITS:  .BYTE          0
1358 006057 000          ADRCNT: .BYTE          0
1359
1360                ; ADVANCE TO NEXT TEST HANDLER
1361                -----
1362
1363 006060 013716 001442      .ADVANCE: MOV     NEXT,(SP) ; CRUNCH STACK WITH ADDRESS OF SCOPE CALL
1364 006064 005037 001444      CLR     LOCK            ; RESET TIGHT LOOP ADDRESS
1365 006070 000002      RTI                    ; CHECK TO SEE IF OLD TEST GETS REPEATED
1366
1367                ; SAVE PC OF TEST THAT FAILED AND RO-R5
1368                -----
1369
1370 006072 016637 000004 001460 .SAVOS: MOV     4(SP),SAVPC ; SAVE R7 (PC)
1371
1372                ; SAVE RO-R5
1373
1374 006100 010537 001274      SVOS:  MOV     R5,$REG5   ; SAVE R5
1375 006104 010437 001272      MOV     R4,$REG4       ; SAVE R4
1376 006110 010337 001270      MOV     R3,$REG3       ; SAVE R3
1377 006114 010237 001266      MOV     R2,$REG2       ; SAVE R2
1378 006120 010137 001264      MOV     R1,$REG1       ; SAVE R1
1379 006124 010037 001262      MOV     R0,$REG0       ; SAVE R0
1380 006130 000002      RTI                    ; LEAVE.
1381
1382                ; RESTORE RO-R5
1383
1384 006132 013700 001262      .RESOS: MOV     $REG0,R0 ; RESTORE R0
1385 006136 013701 001264      MOV     $REG1,R1       ; RESTORE R1
1386 006142 013702 001266      MOV     $REG2,R2       ; RESTORE R2
1387 006146 013703 001270      MOV     $REG3,R3       ; RESTORE R3

```



1444 006406 000000  
1445 006410 000000  
1446 006411 000000  
1447 006412 000000  
1448  
1449  
1450  
1451  
1452  
1453  
1454  
1455  
1456  
1457  
1458  
1459  
1460  
1461  
1462

WROCNT: 0  
CHRCNT: 0  
SPACNT=CHRCNT+1  
BINWRD: 0

: TRAP DISPATCH SERVICE  
: ARGUMENT OF TRAP IS EXTRACTED  
: AND USED AS OFFSET TO OBTAIN POINTER  
: TO SELECTED SUBROUTINE

.SBTTL TRAP DECODER

\*\*\*\*\*  
: \*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION  
: \*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS  
: \*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL  
: \*GO TO THAT ROUTINE.

1463 006414 010046  
1464 006416 016600 000002  
1465 006422 005740  
1466 006424 111000  
1467 006426 006300  
1468 006430 016000 006450  
1469 006434 000200  
1470  
1471  
1472  
1473

\$TRAP: MOV RO, -(SP) ;; SAVE RO  
MOV 2(SP), RO ;; GET TRAP ADDRESS  
TST -(RO) ;; BACKUP BY 2  
MOVB (RO), RO ;; GET RIGHT BYTE OF TRAP  
ASL RO ;; POSITION FOR INDEXING  
MOV \$TRPAD(RO), RO ;; INDEX TO TABLE  
RTS RO ;; GO TO ROUTINE

;; THIS IS USE TO HANDLE THE "GETPRI" MACRO

1474 006436 011646  
1475 006440 016666 000004 000002  
1476 006446 000002  
1477  
1478  
1479  
1480  
1481  
1482  
1483  
1484

\$TRAP2: MOV (SP), -(SP) ;; MOVE THE PC DOWN  
MOV 4(SP), 2(SP) ;; MOVE THE PSW DOWN  
RTI ;; RESTORE THE PSW

.SBTTL TRAP TABLE

: \*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED  
: \*BY THE "TRAP" INSTRUCTION.

1485 006450 006436  
1486 006452 004414  
1487  
1488  
1489 006454 005144  
1490 006456 005264  
1491 006460 005564  
1492 006462 004364  
1493 006464 006072  
1494 006466 006132  
1495 006470 007362  
1496 006472 007332  
1497 006474 007400  
1498 006476 007446  
1499 006500 007512

ROUTINE  
-----  
\$TRPAD: .WORD \$TRAP2  
\$TYPE ;; CALL=TYPE TRAP+1(104401) TTY TYPEOUT ROUTINE  
  
\$RDCHR ;; CALL=RDCHR TRAP+2(104402) TTY TYPEIN CHARACTER ROUTINE  
\$RDLIN ;; CALL=RDLIN TRAP+3(104403) TTY TYPEIN STRING ROUTINE  
\$RDOCT ;; CALL=RDOCT TRAP+4(104404) READ AN OCTAL NUMBER FROM TTY  
.SCOPI ;; CALL=SCOPI TRAP+5(104405) CALL TO LOOP ON CURRENT DATA HANDLER  
.SAVOS ;; CALL=SAVOS TRAP+6(104406) CALL TO REGISTER SAVE ROUTINE  
.RESOS ;; CALL=RESOS TRAP+7(104407) CALL TO REGISTER RESTORE ROUTINE  
.MSTCLR ;; CALL=MSTCLR TRAP+10(104410) CALL TO ISSUE A MASTER CLEAR  
.DELAY ;; CALL=DELAY TRAP+11(104411) CALL TO DELAY  
.ROMCLK ;; CALL=ROMCLK TRAP+12(104412) CALL TO CLOCK ROM ONCE  
.DATACLK ;; CALL=DATACLK TRAP+13(104413) CALL TO CLOCK DATA  
.TIMER ;; CALL=TIMER TRAP+14(104414) CALL TO DELAY A CLOCK TICK

1500	006502	005724			\$INPUT ;;CALL=INPUT TRAP+15(104415) CALL TO OCTAL # INPUT ROUTINE
1501	006504	006164			.CONVRT ;;CALL=CONVRT TRAP+16(104416) CALL TO .....
1502	006506	006170			.CNVRT ;;CALL=CNVRT TRAP+17(104417) CALL TO .....
1503	006510	006060			.ADVANCE ;;CALL=ADVANCE TRAP+20(104420) CALL TO ADVANCE TO NEXT TEST
1504					
1505					
1506					
1507					
1508					
1509					
1510	006512	004737	011212		\$ERROR: JSR PC,CKSWR ;CHECK FOR SOFT SWR
1511	006516	032777	010000	172514	BIT #SW12,2SWR ;BELL ON ERROR?
1512	006524	001406			BEQ XBX ;BR IF NO BELL
1513	006532	105777	172516		TSTB 2STPS ;TTY READY
1514	006532	100003			BPL XBX ;DON'T WAIT IF TTY NOT READY.
1515	006534	112777	000207	172510	MOV #207,2STPB ;PUSH A BELL AT THE TTY.
1516	006542	032777	020000	172470	XBX: BIT #SW13,2SWR ;DELETE ERROR PRINT OUT?
1517	006550	001107			BNE HALTS ;BR IF NO PRINT OUT WANTED.
1518	006552	021637	001216		CMP (SP),SERRPC ;WAS THIS ERROR FOUND LAST TIME?
1519	006556	001404			BEQ IS ;BR IF YES
1520	006560	011637	001216		MOV (SP),SERRPC ;RECORD BEING HERE
1521	006564	105037	001203		CLRB SERFLG ;PREPARE HEADER
1522	006570	104406			IS: SAVOS ;SAVE ALL PROC REGISTERS
1523	006572	011605			MOV (SP),R5 ;GET THE PC OF ERROR
1524	006574	162705	000002		SUB #2,R5 ;GET ADDRESS OF TRAP CALL
1525	006600	011504			MOV (R5),R4 ;GET ERROR INSTRUCTION
1526	006602	110437	001214		MOV R4,\$ITEMB ;COPY ERROR # FOR APT HANDLING
1527	006606	006304			ASL R4 ;MULT BY TWO
1528	006610	061504			ADD (R5),R4 ;DOUBLE IT
1529	006612	006304			ASL R4 ;MULT AGAIN
1530	006614	042704	177001		BIC #177001,R4 ;CLEAR JUNK
1531	006620	062704	001512		ADD #SERRTB,R4 ;GET POINTER
1532	006624	012437	006740		MOV (R4)+,ERRMSG ;GET ERROR MESSAGE
1533	006630	012437	006752		MOV (R4)+,DATAHD ;GET DATA HEADER
1534	006634	011437	006764		MOV (R4),DATABP ;GET DATA TABLE
1535	006640	105737	001203		TSTB SERFLG ;TYPE HEADREER
1536	006644	001403			BEQ TYPMSG ;BR IF YES
1537	006646	005737	006764		TST DATABP ;DOES DATA TABLE EXIST?
1538	006652	001040			BNE TYPDAT ;BR IF YES.
1539	006654	104401	001313		TYPMSG: TYPE ,SCLF
1540	006660	104401	001313		TYPE ,SCLF
1541	006664	005737	001444		TST LOCK
1542	006670	001402			BEQ IS
1543	006672	104401	010015		TYPE ,MASTEK
1544	006676	104401	010003		IS: TYPE ,MTSTN
1545	006702	104417	007120		CNVRT ,XTSTN ;SHOW IT
1546	006706	104401	010072		TYPE ,MERRPC ;TYPE PC.
1547	006712	104417	007112		CNVRT ,ERTABO ;SHOW IT
1548	006716	104401	001313		TYPE ,SCLF ;GIVE A CR/LF
1549	006722	112737	177777	001203	MOV #-1,SERFLG ;NO MORE HEADER UNLESS NO DATA TABLE.
1550	006730	005737	006740		TST ERRMSG ;IS THERE AN ERROR MESSAGE?
1551	006734	001402			BEQ WRKO.FM ;BR IF NO.
1552	006736	104401			TYPE ;TYPE
1553	006740	000000			ERRMSG: 0 ;ERROR MESSAGE
1554	006742				WRKO.FM: ;
1555	006742	005737	006752		TST DATAHD ;DATA HEADER?

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1556 006746 001402          BEQ      TYPDAT      ; BR IF NO
1557 006750 104401          TYPE
1558 006752 000000          DATAHD: 0          ; DATA HEADER
1559 006754 005737 006764      TYPDAT: TST      DATABP ; DATA TABLE?
1560 006760 001402          BEQ      RESREG      ; BR IF NO.
1561 006762 104416          CONVRT ; SHOW
1562 006764 000000          DATABP: 0          ; DATA TABLE
1563 006766 104407          RESREG: RESOS      ; RESTORE PROC REGISTERS
1564 006770 122737 000001 001336 HALTS:  CMPB      #APTENV, $ENV ; IS APT RUNNING ?
1565 006776 001007          BNE      3$          ; SKIP APT CALL IF NOT.
1566 007000 113737 001214 007012      MOVB     $ITEMB, 6$ ; COPY ERROR #.
1567 007006 004737 004714          JSR      PC, $ATY4   ; CALL APT SERVICES.
1568 007012 000000          6$:      WORD      0          ; ERROR # GOES HERE.
1569 007014 000777          9$:      BR        9$          ; LOCK HERE.
1570 007016 022737 004070 000042      3$:      CMP      #SENDAD, @#42 ; IF ACT-11 AUTOMATIC MODE, HALT!!
1571 007024 001403          BEQ      1$          ;
1572 007026 005777 172206      TST     @SWR          ; HALT ON ERROR?
1573 007032 100005          BPL     EXITER       ; BR IF NO HALT ON ERROR
1574 007034 010046          1$:     PUSHRO ; SAVE R0
1575 007036 016600 000002      MOV     2(SP), R0    ; SHOW ERROR PC IN DATA LIGHTS
1576 007042 000000          HALT
1577 007044 012600          POPRO  ; GET R0
1578 007046 005237 001212      EXITER: INC     $ERTTL ; UPDATE ERROR COUNT
1579 007052 032777 000400 172160      BIT     #SW08, @SWR ; GOTO TOP OF TEST?
1580 007060 001007          BNE     1$          ; BR IF YES
1581 007062 032777 002000 172150      BIT     #SW10, @SWR ; GOTO NEXT TEST?
1582 007070 001407          BEQ     2$          ; BR IF NO
1583 007072 013737 001442 001206      MOV     NEXT, $LPADR ; SET FOR NEXT TEST
1584 007100 012706 001200      1$:     MOV     #STACK, SP ; RESET SP
1585 007104 000177 172076          JMP     @SLPADR      ; GOTO SPECIFIED TEST
1586 007110 000002          2$:     RTI          ; $LPADR
1587 007112 000001          ERTAB0: 1
1588 007114          006      002          .BYTE   6, 2
1589 007116 001460          SAVPC
1590 007120 000001          XTSTN: 1
1591 007122          003      002          .BYTE   3, 2
1592 007124 001202          $TSTNM
1593          ; ENTER HERE ON POWER FAILURE
1594          ; -----
1595
1596          .SBTTL  POWER DOWN AND UP ROUTINES
1597
1598          ; *****
1599          ; POWER DOWN ROUTINE
1600 007126 012737 007316 000024 $PWRDN: MOV     #SILLUP, @#PWRVEC ; SET FOR FAST UP
1601 007134 012737 000340 000026      MOV     #340, @#PWRVEC+2 ; PRIO:7
1602 007142 010046          MOV     7, -(SP)    ; PUSH R0 ON STACK
1603 007144 010146          MOV     1, -(SP)    ; PUSH R1 ON STACK
1604 007146 010246          MOV     R2, -(SP)   ; PUSH R2 ON STACK
1605 007150 010346          MOV     R3, -(SP)   ; PUSH R3 ON STACK
1606 007152 010446          MOV     R4, -(SP)   ; PUSH R4 ON STACK
1607 007154 010546          MOV     R5, -(SP)   ; PUSH R5 ON STACK
1608 007156 017746 172056      MOV     @SWR, -(SP) ; PUSH @SWR ON STACK
1609 007162 010637 007322          MOV     SP, $SAVR6 ; SAVE SP
1610 007166 012737 007200 000024      MOV     #SPWRUP, @#PWRVEC ; SET UP VECTOR
1611 007174 000000          HALT

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1612 007176 000776          BR      .-2          ;; HANG UP
1613
1614          ;; *****
1615          : POWER UP ROUTINE
1616 007200 012737 007316 000024 $PHRUP: MOV      $SILLUP, @PHRVEC  ;; SET FOR FAST DOWN
1617 007206 013706 007322          MOV      $SAVR6, SP      ;; GET SP
1618 007212 005037 007322          CLR      $SAVR6          ;; WAIT LOOP FOR THE TTY
1619 007216 005237 007322          IS:   INC      $SAVR6      ;; WAIT FOR THE INC
1620 007222 001375          BNE     IS                ;; OF WORD
1621 007224 104401 007562          TYPE   ,MPFAIL
1622 007230 104417 007324          CMVRT  ,PFTAB
1623 007234 105037 001203          CLR    $ERFLG          ;; CLEAR ERROR FLAG.
1624 007240 005037 001216          CLR    $ERRPC          ;; CLEAR LAST ERROR PC
1625 007244 013701 002066          MOV    $MCSR, R1      ;; RESTORE DEVICE ADDRESS.
1626 007250 005011          CLR    (R1)           ;; CLEAR THE CSR.
1627 007252 104410          MSTCLR
1628 007254 012677 171760          MOV    (SP)+, @R4      ;; POP STACK INTO R4
1629 007260 012605          MOV    (SP)+, @R5      ;; POP STACK INTO R5
1630 007262 012604          MOV    (SP)+, @R4      ;; POP STACK INTO R4
1631 007264 012603          MOV    (SP)+, @R3      ;; POP STACK INTO R3
1632 007266 012602          MOV    (SP)+, @R2      ;; POP STACK INTO R2
1633 007270 012601          MOV    (SP)+, @R1      ;; POP STACK INTO R1
1634 007272 012600          MOV    (SP)+, @R0      ;; POP STACK INTO R0
1635 007274 012737 007126 000024          MOV    $SPWRDN, @PHRVEC ;; SET UP THE POWER DOWN VECTOR
1636 007302 012737 000340 000026          MOV    @340, @PHRVEC+2 ;; @R0:7
1637 007310 104401          TYPE   ,MPFAIL        ;; REPORT THE POWER FAILURE
1638 007312 007562          $PHRNG: .WORD MPFAIL  ;; POWER FAIL MESSAGE POINTER
1639 007314 000002          RTI
1640 007316 000000          $SILLUP: HALT
1641 007320 000776          BR      .-2          ;; THE POWER UP SEQUENCE WAS STARTED
1642 007322 000000          $SAVR6: 0            ;; BEFORE THE POWER DOWN WAS COMPLETE
1643          ;; PUT THE SP HERE
1644 007324 000001          PFTAB: 1
1645 007326 003 002          .BYTE 3,2
1646 007330 001202          .STNM
1647
1648 007332          .DELAY:
1649 007332 012777 000020 172534          MOV    @20, @KMP04
1650 007340 104412          ROMCLK 121111          ;; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1651 007342 121111          IS:   ROMCLK 121224          ;; POKE CLOCK DELAY BIT
1652 007344          ;; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1653 007344 104412          ROMCLK 121224          ;; PORT4+IBUS#11
1654 007346 121224          BIT    @BIT4, @KMP04   ;; IS CLOCK BIT SET?
1655 007350 032777 000020 172516          BEQ    IS                ;; BR IF NO
1656 007356 001772          RTI
1657 007360 000002
1658
1659 007362          .MSTCLR:
1660 007362 152777 000100 172500          BISB  @BIT6, @MCSRH    ;; SET MASTER CLEAR
1661 007370 142777 000300 172472          BICB  @BIT6!BIT7, @MCSRH ;; CLEAR MASTER CLEAR AND RUN
1662 007376 000002          RTI                ;; RETURN
1663
1664 007400          .ROMCLK:
1665 007400 152777 000002 172462          BISB  @BIT1, @MCSRH    ;; SET ROMI
1666 007406 013677 172464          MOV    @2(SP)+, @KMP06 ;; LOAD INSTRUCTION IN SEL6
1667 007412 062746 000002          ADD   @2, -(SP)        ;; ADJUST STACK
    
```

```

1668 007416 032777 000100 171614 BIT #SW06,2SWR ;HALT IF SW06 =1
1669 007424 001401 BEQ 15 ;BR IF SW06 =0
1670 007426 000000 HALT ;HALT BEFORE CLOCKING INSTRUCTION
1671 007430 152777 000003 172432 1S: BISB #BIT1!B. )2KMC5RH ;CLOCK INSTRUCTION
1672 007436 142777 000007 172424 BICB #BIT2!BIT1!BIT0,2KMC5RH ;CLEAR ROM0, ROM1, STEP
1673 007444 000002 RTI
1674
1675 007446 .DATACLK:
1676 007446 013637 011106 MOV 2(SP)+,TEMP ;PUT TICK COUNT IN TEMP
1677 007452 062746 000002 ADD #2,-(SP) ;ADJUST STACK
1678 007456 152777 000020 172404 1S: BISB #BIT4,2KMC5RH ;SET STEP LU
1679 007464 027777 172376 172374 CMP 2KMC5R,2KMC5R ;WASTE TIME
1680 007472 142777 000020 172370 BICB #BIT4,2KMC5RH ;CLEAR STEP LU
1681 007500 005337 011106 DEC TEMP ;DEC TICK COUNT
1682 007504 001364 BNE 15 ;BR IF NOT DONE
1683 007506 000002 RTI ;RETURN
1684 007510 000001 3S: .BLKW 1
1685
1686 007512 .TIMER:
1687 007512 013637 011106 MOV 2(SP)+,TEMP ;MOVE COUNT TO TEMP
1688 007516 062746 000002 ADD #2,-(SP) ;ADJUST STACK
1689 007522 1S:
1690 007522 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1691 007524 021364 021364 PORT4+IBUS* REG11 ;PORT4+IBUS* REG11
1692 007526 032777 000002 172340 BIT #2,2KMP04 ;IS PGM CLOCK BIT CLEAR?
1693 007534 001772 BEQ 15 ;BR IF YES
1694 007536 2S:
1695 007536 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1696 007540 021364 021364 PORT4+IBUS* REG11 ;PORT4+IBUS* REG11
1697 007542 032777 000002 172324 BIT #2,2KMP04 ;IS PGM CLOCK BIT SET?
1698 007550 001372 BNE 2S ;BR IF YES
1699 007552 005337 011106 DEC TEMP ;DEC COUNT
1700 007556 001361 BNE 15 ;BR IF NOT DONE
1701 007560 000002 RTI ;RETURN
1702
1703 007562 050200 051127 043040 MPFAIL: .ASCIZ <200>/PWR FAILED. RESTART AT TEST /
( ) 007620 042600 042116 050040 MPASS: .ASCIZ <200>/END PASS LZKCD /
( ) 007642 051200 000 MR: .ASCIZ <200>/R/
( ) 007645 200 047516 042040 MERR2: .ASCIZ <200>/NO DEVICES PRESENT./
( ) 007672 044600 051516 043125 MERR3: .ASCIZ <200>/INSUFFICIENT DATA! /
( ) 007716 046200 041517 020113 MLOCK: .ASCIZ <200>/LOCK ON SELECTED TEST/
( ) 007745 103 051123 020072 MCSRX: .ASCIZ /CSR: /
( ) 007753 126 041505 020072 MVECX: .ASCIZ /VEC: /
( ) 007761 120 051501 042523 MPASSX: .ASCIZ /PASSES: /
( ) 007772 051105 047522 051522 MERRX: .ASCIZ /ERRORS: /
( ) 010003 124 051505 020124 MTSTN: .ASCIZ /TEST NO: /
( ) 010015 052 000 MASTEX: .ASCIZ /*/
( ) 010017 200 042523 020124 MNEW: .ASCIZ <200>/SET SWITCH REG TO KMC11'S DESIRED ACTIVE./
( ) 010072 041520 020072 000 MERRPC: .ASCIZ /PC: /
( ) 010077 200 020040 020040 XHEAD: .ASCII <200>/
( ) 010136 020200 020040 020040 .ASCII <200>/
( ) 010175 200 020040 041520 .ASCII <200>/ PC CSR STAT1 STAT2 STAT3/
( ) 010247 200 026455 026455 .ASCII <200>/-----
( ) 010323 200 047510 020127 NUM: .ASCIZ <200>/HOW MANY KMC11'S TO BE TESTED?/
( ) 010363 200 051503 020122 CSR: .ASCIZ <200>/CSR ADDRESS?/
( ) 010401 200 042526 052103 VEC: .ASCIZ <200>/VECTOR ADDRESS?/

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POWER DOWN AND UP ROUTINES

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(2) 010422 041200 020122 051120 PRIO: .ASCIZ <200>/BR PRIORITY LEVEL? (4 5 6 7)?/
(2) 010461 200 044127 041511 MODU: .ASCIZ <200>/WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYP
(2) 010573 200 053523 052111 LINE: .ASCIZ <200>/SWITCH PAC#1 (DOCMP LINE #)?/
(2) 010631 200 053523 052111 BM: .ASCIZ <200>/SWITCH PAC#2 (BM873 BOOT ADD)?/
(2) 010671 200 051511 052040 CONN: .ASCIZ <200>/IS THE LOOP BACK CONNECTOR ON?/
(2) 010731 200 047516 042040 NOACT: .ASCIZ <200>/NO DEVICES ARE SELECTED/
(2) 010762 100200 046513 030503 CONERR: .ASCIZ <200><200>/KMC11 AT NONSTANDARD ADDRESS PC: /
(2) 011027 200 054105 042520 CNERR: .ASCIZ <200>/EXPECTED FOUND/
(2) 011050 024040 046513 024503 KMCN: .ASCIZ / (KMC) /
(2) .EVEN
(2) 011060 000005 XSTATQ: 5
1704 011062 006 003 .BYTE 6,3
1705 011064 001276 $TMP0
1706 011066 006 003 .BYTE 6,3
1707 011070 001300 $TMP1
1708 011072 006 003 .BYTE 6,3
1709 011074 001302 $TMP2
1710 011076 006 003 .BYTE 6,3
1711 011100 001304 $TMP3
1712 011102 006 002 .BYTE 6,2
1713 011104 001306 $TMP4
1714 .EVEN
1715 ;BUFFERS FOR INPUT-OUTPUT
1716
1717
1718 011106 000000 TEMP: 0
1719 011150 .=. +40
1720 011150 000000 MDATA: 0
1721 011212 .=. +40
1722
1723
1724 ;ROUTINE USED TO CHANGE SOFTWARE SWITCH
1725 ;REGISTER USING THE CONSOLE TERMINAL
1726 -----
1727
1729 011212 022737 000176 001240 CKSWR: CMP #SWREG, SWR ; IS THE SOFT SWR BEING USED?
1729 011220 001075 BNE CKSWRS ; BR IF NO
1730 011222 132737 000001 001336 BITB #1, SENV ; IS IT RUNNING UNDER APT?
1731 011230 001071 BNE CKSWRS ; EXIT IF YES.
1732 011232 022777 000007 170006 CMP #7, 2STKB ; WAS CTRL G TYPED? (7 BIT ASCII)
1733 011240 001404 BEQ 1$ ; BR IF YES
1734 011242 022777 000207 167776 CMP #207, 2STKB ; WAS CTRL G TYPED? (8 BIT ASCII)
1735 011250 001061 BNE CKSWRS ; BR IF NO
1736 011252 010246 1$: MOV R2, -(SP) ; STORE R2
1737 011254 010346 MOV R3, -(SP) ; STORE R3
1738 011256 010446 MOV R4, -(SP) ; STORE R4
1739 011260 012737 177777 011416 MOV #-1, SWFLG ; SET SOFT TYPE OUT FLAG
1740 011266 005002 CKSWR1: CLR R2 ; CLEAR NEW SWR CONTENTS
1741 011270 012704 177777 MOV #-1, R4 ; SET FLAG TO ALL ONES
1742 011274 104401 005541 TYPE , SM$WR ; TYPE "SWR="
1743 011300 104417 CKSWR2: CNVRT ; TYPE OUT PRESENT CONTENTS
1744 011302 011452 SOFTSW ; OF SOFT SWITCH REGISTER
1745 011304 104401 005552 CKSWR3: TYPE , SMNEW ; TYPE "NEW="
1746 011310 004737 011420 CKSWR4: JSR PC, INCHAR ; GET RESPONSE
1747 011314 022703 000015 CMP #15, R3 ; WAS IT A CR?
1748 011320 001424 BEQ 5$ ; BR IF YES

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1786
1787
1788
1789
1790
1791
1792
1793
1794
1795 011460 005737 001470          CYCLE: TST      KMACTV      ;ARE ANY KMC11'S TO BE TESTED?
1796 011464 001004                    BNE      1$          ;BR IF OK.
1797 011466 104401 010731          TYPE     ,NOACT     ;NO KMC11'S SELECTED!!
1798 011472 000000                    HALT                    ;STOP THE SHOW.
1799 011474 000776                    BR                          ;DISQUALIFY CONT. SW.
1800 011476 000241          1$: CLC          ;CLEAR PROC. CARRY BIT.
1801 011500 006137 001500          ROL      RUN        ;UPDATE POINTER
1802 011504 005537 001500          ADC      RUN        ;CATCH CARRY FROM RUN
1803 011510 062737 000004 001504          ADD     #4,MILK     ;UPDATE POINTER
1804 011516 062737 000010 001502          ADD     #10,CREAM   ;UPDATE ADDRESS POINTER.
1805 011524 022737 002300 001502          CMP     #KM.MAP+200,CREAM
1806 011532 001006                    BNE      2$          ;KEEP GOING; NOT ALL TESTED FOR.
1807 011534 012737 002100 001502          MOV     #KM.MAP,CREAM ;RESET ADDRESS POINTER.
1808 011542 012737 002302 001504          MOV     #CNT.MAP,MILK ;RESET PASS COUNT POINTER
1809 011550 033737 001500 001470 2$: BIT     RUN,KMACTV ;IS THIS ONE ACTIVE?
1810 011556 001747                    BEQ     1$          ;BR IF NO
1811 011560 013700 001502          MOV     CREAM,R0    ;GET ADDRESS POINTER
1812 011564 013702 001504          MOV     MILK,R2     ;GET PASS COUNT POINTER
1813 011570 012037 002066          MOV     (R0)+,KMCSR ;LOAD SYSTEM CTRL. REG
1814 011574 011037 002056          MOV     (R0),KMRVEC ;LOAD VECTOR
1815 011600 042737 177000 002056          BIC     #177000,KMRVEC ;CLEAR UNWANTED BITS
1816 011606 012037 002050          MOV     (R0)+,STAT1 ;LOAD STAT1
1817 011612 012037 002052          MOV     (R0)+,STAT2 ;LOAD STAT2
1818 011616 012037 002054          MOV     (R0)+,STAT3 ;LOAD STAT3
1819 011622 012237 001324          MOV     (R2)+,SPASS ;LOAD PASS COUNT
1820 011626 012237 001212          MOV     (R2)+,SERTL ;LOAD ERROR COUNT
1821 011632 012700 000002          MOV     #2,R0       ;SAVE CORE THIS WAY!
1822 011636 013737 002066 002070          MOV     KMCSR,KMCSRH
1823 011644 005237 002070          INC     KMCSRH
1824 011650 013737 002070 002072          MOV     KMCSRH,KMCTL
1825 011656 005237 002072          INC     KMCTL
1826 011662 013737 002072 002074          MOV     KMCTL,KMP04
1827 011670 060037 002074          ADD     R0,KMP04
1828 011674 013737 002074 002076          MOV     KMP04,KMP06
1829 011702 060037 002076          ADD     R0,KMP06
1830
1831 011706 013737 002056 002060          MOV     KMRVEC,KMRLVL ;PTY LVL
1832 011714 060037 002060          ADD     R0,KMRLVL
1833 011720 013737 002060 002062          MOV     KMRLVL,KMTVEC ;TX VEC
1834 011726 060037 002062          ADD     R0,KMTVEC
1835 011732 013737 002062 002064          MOV     KMTVEC,KMTLVL ;TX LVL
1836 011740 060037 002064          ADD     R0,KMTLVL
1837
1838 011744 032737 000002 001446          BIT     #SW01,STRTSW ;IS TEST NO. SELECTED
1839 011752 001447                    BEQ     7$          ;BR IF NO
1840 011754
1841 011754 005737 000042          4$: TST     #42          ;RUNNING IN AUTO MODE?
    
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1842 011760 001044      BNE      7$          ;BR IF YES
1843 011762 104401 001313  TYPE      ,SRLF
1844 011766 104415      INPUT
1845 011770 010003      MTSTN
1846 011772 000001      1
1847 011774 001000      1000
1848 011776 001202      $STNM
1849 012000      000      .BYTE
1850 012001      001      .BYTE
1851 012002 012700 013732  MOV      #TST1,R0
1852 012006 022710 5$:      CMP      (PC)+,(R0) ;CMP FIRST WORD TO 12737
1853 012010 012737      MOV      (PC)+,2(PC)+
1854 012012 001020      BNE      6$          ;BR IF NOT SAME
1855 012014 023760 001202 000002  CMP      $STNM,2(R0) ;DOES $STNM MATCH?
1856 012022 001014      BNE      6$          ;BR IF NO
1857 012024 022760 001202 000004  CMP      #STNM,4(R0) ;IS LAST WORD OK?
1858 012032 001010      BNE      6$          ;BR IF NO
1859 012034 010037 001206      MOV      R0,$LPADR ;IT IS A LEGAL TEST SO DO IT
1860 012040 104401 007642      TYPE      MR
1861 012044 042737 000002 001446  BIC      #SW01,STRTSW
1862 012052 000412      BR
1863 012054 005720 6$:      TST      (R0)+      ;POP R0
1864 012056 020027 020634  CMP      R0,#TLAST+10 ;AT END YET?
1865 012062 001351      BNE      5$          ;BR IF NO
1866 012064 104401 001312  TYPE      $QUES      ;YES ILLEGAL TEST NO.
1867 012070 000731      BR      4$          ;TRY AGAIN
1868
1869 012072 012737 013732 001206 7$:      MOV      #TST1,$LPADR ;PREPARE $LPADR ADDRESS
1870 012100 013701 002066 8$:      MOV      KMC11,R1    ;R1 = BASE KMC11 ADDRESS
1871 012104 000177 167076  JMP      2$LPADR    ;GO START TESTING.
1872
1873
1874      ;ROUTINE USED TO "AUTO SIZE" THE KMC11
1875      ;CSR AND VECTOR.
1876      ;NOTE: THE CSR MAY BE ANY WHERE IN THE FLOATING
1877      ;ADDRESS RANGE (160000:164000)
1878      ;AND THE VECTOR MAY BE ANY WHERE IN THE
1879      ;FLOATING VECTOR RANGE (300:770)
1880      ;
1881      ;
1882      AUTO.SIZE:
1883 012110 000005      RESET
1884 012112 012702 002100  CSRMAP: MOV      #KM.MAP,R2 ;INSURE A BUS INIT.
1885 012116 005022      CLR      (R2)+      ;LOAD MAP POINTER.
1886 012120 022702 002300  1$:      CMP      #KM.END,R2 ;ZERO ENTIRE MAP
1887 012124 001374      BNE      1$          ;ALL DONE?
1888 012126 005037 001472  CLR      KMINUM      ;SET OCTAL NUMBER OF KMC11'S TO 0
1889 012132 012702 002100  MOV      #KM.MAP,R2 ;R2 POINTS TO KMC MAP
1890 012136 005037 001470  CLR      KMACTV      ;CLEAR ACTIVE
1891 012142 032737 000001 001446  BIT      #SW00,STRTSW ;QUESTIONS?
1892 012150 001002      BNE      .+6         ;BR IF YES
1893 012152 000177 012532  JMP      7$          ;IF NO SKIP QUESTIONS
1894 012156 012737 000001 001306  MOV      #1,$TMP4    ;START WITH 1
1895 012164 104415      INPUT
1896 012166 010323      NUM
1897 012170 000001      1

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1898	012172	000020				16.			
1899	012174	001302				STMP2			
1900	012176	000				.BYTE	0		
1901	012177	001				.BYTE	1		
1902	012200	013737	001302	001472		MOV	STMP2,KMNUM	;KMNUM = HOW MANY	
1903	012206	104401	001313		12\$:	TYPE	,SCRLF		
1904	012212	104416				CONVRT		;TYPE WHICH KMC IS BEING DONE	
1905	012214	013164				WHICH		;STMP4 IS WHICH KMC	
1906	012216	005237	001306			INC	STMP4		
1907	012222	104415				INPUT			
1908	012224	010363				CSR			
1909	012226	160000				160000			
1910	012230	164000				164000			
1911	012232	001304				STMP3			
1912	012234	000				.BYTE	0		
1913	012235	001				.BYTE	1		
1914	012236	013722	001304			MOV	STMP3,(R2)+	;STORE CSR IN MAP	
1915	012242	104415				INPUT			
1916	012244	010401				VEC			
1917	012246	000000				0			
1918	012250	000776				776			
1919	012252	001304				STMP3			
1920	012254	000				.BYTE	0		
1921	012255	001				.BYTE	1		
1922	012256	013712	001304			MOV	STMP3,(R2)	;STORE VECTOR IN MAP	
1923	012262	104401			10\$:	TYPE			
1924	012264	010422				PRI0		;ASK WHAT BR LEVEL	
1925	012266	004737	013456			JSR	PC,INTTY	;GET RESPONSE	
1926	012272	022703	000024			CMP	#24,R3		
1927	012276	101014				BHI	50\$	;BR IF LESS THAN 4	
1928	012300	022703	000027			CMP	#27,R3		
1929	012304	103411				BLO	50\$	;BR IF GREATER THAN 7	
1930	012306	012704	000011			MOV	#11,R4	;R4 = NUMBER OF SHIFTS	
1931	012312	006303				ASL	R3	;SHIFT R3 LEFT	
1932	012314	005304				DEC	R4	;DEC SHIFT COUNT	
1933	012316	001375				BNE	.-4	;BR IF NOT DONE	
1934	012320	042703	170777			BIC	#170777,R3	;BIC UNWANTED BITS	
1935	012324	050312				BIS	R3,(R2)	;PUT BR LEVEL IN STATUS MAP	
1936	012326	000403				BR	8\$	;CONTINUE	
1937	012330	104401			50\$:	TYPE			
1938	012332	001312				\$QUES		;RESPONSE IS OUT OF LIMITS	
1939	012334	000752				BR	10\$	;TRY AGAIN	
1940	012336				8\$:				
1941	012336				9\$:				
1942	012336	104401			16\$:	TYPE			
1943	012340	010461				MODU		;ASK WHICH LINE UNIT	
1944	012342	004737	013456			JSR	PC,INTTY	;GET REPLY	
1945	012346	022703	000021			CMP	#21,R3	; "1"	
1946	012352	001417				BEQ	30\$		
1947	012354	022703	000022			CMP	#22,R3	; "2"	
1948	012360	001412				BEQ	31\$		
1949	012362	022703	000116			CMP	#116,R3	; "N"	
1950	012366	001403				BEQ	32\$		
1951	012370	104401				TYPE			
1952	012372	001312				\$QUES		;IF NOT A 1,2 OR N TYPE ""	
1953	012374	000760				BR	16\$	;TRY AGAIN	

POWER DOWN AND UP ROUTINES

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1954 012376 052722 010000 32$: BIS #BIT12,(R2)+ ;SET BIT 12 IN STAT2 IF NO LU
1955 012402 052222 010000 CMP (R2)+,(R2)+ ;POP OVER STAT2 AND STAT3
1956 012404 000445 010000 BR 33$
1957 012406 052712 020000 31$: BIS #BIT13,(R2) ;SET BIT 13 IN STAT2 IF M8202
1958 012412 104401 010000 30$: TYPE
1959 012414 010671 010000 CONN ;ASK IF LOOP-BACK IS ON
1960 012416 004737 013456 JSR PC,INTTY ;GET REPLY
1961 012422 022703 000131 CMP #131,R3 ;Y
1962 012426 001406 010000 BEQ 17$
1963 012430 022703 000116 CMP #116,R3 ;N
1964 012434 001406 010000 BEQ 18$
1965 012436 104401 010000 TYPE
1966 012440 001312 010000 SQUES ;IF NOT Y OR N TYPE "?"
1967 012442 000763 010000 BR 30$ ;TRY AGAIN
1968 012444 052722 040000 17$: BIS #BIT14,(R2)+ ;TURNAROUND IS CONNECTED
1969 012450 000402 010000 BR 19$
1970 012452 042722 040000 18$: BIC #BIT14,(R2)+ ;NO TURNAROUND
1971 012456 010000 19$:
1972 012456 104415 010000 INPUT
1973 012460 010573 010000 LINE
1974 012462 000000 010000 0
1975 012464 000377 010000 377
1976 012466 001304 010000 $TMP3
1977 012470 000 010000 .BYTE 0
1978 012471 001 010000 .BYTE 1
1979 012472 113722 001304 MOVB $TMP3,(R2)+ ;STORE SWITCH PAC IN MAP
1980 012476 104415 010000 INPUT
1981 012500 010631 010000 BM
1982 012502 000000 010000 0
1983 012504 000377 010000 377
1984 012506 001304 010000 $TMP3
1985 012510 000 010000 .BYTE 0
1986 012511 001 010000 .BYTE 1
1987 012512 113722 001304 MOVB $TMP3,(R2)+ ;STORE SWITCH PAC IN MAP
1988 012516 005722 010000 TST (R2)+ ;POP OVER STAT3
1989 012520 005337 001302 33$: DEC $TMP2 ;DEC KMC COUNT
1990 012524 001230 010000 BNE 12$ ;BR IF MORE TO DO
1991 012526 000137 013064 JMP 13$ ;CONTINUE
1992 012532 012701 160000 7$: MOV #160000,R1 ;SET FOR FIRST ADDRESS TO BE TESTED
1993 012536 012737 013156 000004 2$: MOV #652#4,R1 ;SET FOR NON-EXISTANT DEVICE TIME OUT
1994 012544 005011 010000 CLR (R1) ;CLEAR SEL0
1995 012546 005711 010000 TST (R1) ;IF KMC11 KMCSR S/B 0
1996 012550 001135 010000 BNE 3$ ;IF NO DEV ; TRAP TO 4. IF NO BIT 8 THEN NO KMC11
1997 012552 005061 000006 CLR 6(R1) ;CLEAR SEL6
1998 012556 005761 000006 TST 6(R1) ;IF KMC11 THEN KMRIC S/B =0!
1999 012562 001130 010000 BNE 3$ ;BR IF NOT KMC11
2000 012564 012711 002000 MOV #BIT10,(R1) ;SET ROM0
2001 012570 005061 000004 CLR 4(R1) ;CLEAR SEL4
2002 012574 012761 125252 000006 MOV #125252,6(R1) ;WRITE THIS TO SEL6
2003 012602 052711 020000 BIS #BIT13,(R1) ;WRITE IT!
2004 012606 022761 125252 000004 CMP #125252,4(R1) ;WAS IT WRITTEN?
2005 012614 001113 010000 BNE 3$ ;IF NO IT IS NOT CRAM
2006 ;AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A KMC11 CSR ADDRESS.
2007 012616 010122 010000 21$:
2008 012616 010122 010000 22$: MOV R1,(R2)+ ;STORE CSR IN CORE TABLE.
2009 012620 012711 001000 15$: MOV #BIT9,(R1) ;CLEAR LINE UNIT LOOP
    
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2010	012624	005061	000004		CLR	4(R1)	; CLEAR PORT4
2011	012630	012761	122113	000006	MOV	#122113,6(R1)	; LOAD INSTRUCTION (CLR DTR)
2012	012636	052711	000400		BIS	#BIT8,(R1)	; CLOCK INSTRUCTION
2013	012642	012761	021264	000006	MOV	#021264,6(R1)	; LOAD INSTRUCTION
2014	012650	052711	000400		BIS	#BIT8,(R1)	; CLOCK INSTRUCTION
2015	012654	122761	000377	000004	CMPB	#377,4(R1)	; IS IT ALL ONES?
2016	012652	001003			BNE	.+10	; BR IF NO
2017	012664	052712	010000		BIS	#BIT12,(R2)	; IF YES, NO LINE UNIT, SET STATUS BIT
2018	012670	000436			BR	20\$	
2019	012672	032761	000002	000004	BIT	#BIT1,4(R1)	; IS SWITCH A ONE?
2020	012700	001403			BEQ	.+10	; BR IF M8201
2021	012702	052712	060000		BIS	#BIT13:BIT14,(R2)	; M8202 ASSUME CONNECTOR
2022	012706	000427			BR	20\$	; CONNECTOR ON)
2023	012710	032761	000010	000004	BIT	#BIT3,4(R1)	; IS MRDY SET
2024	012716	001023			BNE	20\$	; BR IF M8201 NO CONNECTOR (ON LINE)
2025	012720	012761	000100	000004	MOV	#BIT6,4(R1)	; LOAD PORT4
2026	012726	012761	122113	000006	MOV	#122113,6(R1)	; LOAD INSTRUCTION
2027	012734	052711	000400		BIS	#BIT8,(R1)	; CLOCK INSTRUCTION(SET DTR)
2028	012740	012761	021264	000006	MOV	#021264,6(R1)	; LOAD INSTRUCTION
2029	012746	052711	000400		BIS	#BIT8,(R1)	; CLOCK INSTRUCTION(READ MODEM REG)
2030	012752	032761	000010	000004	BIT	#BIT3,4(R1)	; IS MRDY SET NOW?
2031	012760	001402			BEQ	20\$	; BR IF NO CONNECTOR
2032	012762	052712	040000		BIS	#BIT14,(R2)	; SET STATUS BIT FOR CONNECTOR
2033	012766	005722			TST	(R2)+	; POP POINTER
2034	012770	012761	021324	000006	MOV	#021324,6(R1)	; PUT INSTRUCTION IN PORT6
2035	012776	012711	001400		MOV	#BIT9:BIT8,(R1)	; PORT4+LU IS
2036	013002	156122	000004		BISB	4(R1),(R2)+	; STORE DDCMP LINE # IN TABLE
2037	013006	012761	021344	000006	MOV	#021344,6(R1)	; PORT6+INSTRUCTION
2038	013014	012711	001400		MOV	#BIT8:BIT9,(R1)	; CLOCK INSTR.
2039	013020	156122	000004		BISB	4(R1),(R2)+	; STORE #M873 ADD IN TABLE
2040	013024	005722			TST	(R2)+	; POP OVER STAT3
2041	013026	005011			CLR	(R1)	; CLEAR ROMI
2042	013030	005237	001472		INC	KMNUM	; UPDATE DEVICE COUNTER
2043	013034	022737	000020	001472	CMP	#20,KMNUM	; ARE MAX. NO. OF DEV FOUND?
2044	013042	001410			BEQ	13\$	; YES DON'T LOOK FOR ANY MORE.
2045	013044	005011			CLR	(R1)	; CLEAR BIT 10
2046	013046	005061	000006		CLR	6(R1)	; CLEAR SEL 6
2047	013052	062701	000010		ADD	#10,R1	; UPDATE CSR POINTER ADDRESS
2048	013056	022701	164000		CMP	#164000,R1	
2049	013062	001230			BNE	2\$	; BR IF MORE ADDRESS TO CHECK.
2050	013064	005037	001470		CLR	KMACTV	
2051	013070	005737	001472		TST	KMNUM	; WERE ANY KMC11'S FOUND AT ALL?
2052	013074	001423			BEQ	5\$	; ERROR AUTO SIZER FOUND NO KMC11'S IN THIS SYS.
2053	013076	013701	001472		MOV	KMNUM,R1	
2054	013102	010137	001476		MOV	R1,SAVNUM	; SAVE NUMBER OF DEVICES
2055	013106	000241			CLC		
2056	013110	006137	001470		ROL	KMACTV	; GENERATE ACTIVE REGISTER OF DEVICES.
2057	013114	005237	001470		INC	KMACTV	; SET THE BIT
2058	013120	005301			DEC	R1	
2059	013122	001371			BNE	4\$	; BR IF MORE TO GENERATE
2060	013124	012737	000006	000004	MOV	#6,2#4	; RESTORE TRAP VECTOR
2061	013132	013737	001470	001474	MOV	KMACTV,SAVACT	; SAVE ACTIVE REGISTER
2062	013140	000137	013172		JMP	VECMAP	; GO FIND THE VECTOR NOW
2063	013144	104401	007645		TYPE	#ERR2	; NOTIFY OPR THAT NO KMC11'S FOUND.
2064	013150	005000			CLR	RO	; MAKE DATA LIGHTS ZERO
2065	013152	000000			HALT		; STOP THE SHOW

2066	013154	000776				BR	.-2		;DISABLE CONT. SW.
2067	013156	012716	013052		6S:	MOV	#14S,(SP)		;ENTERED BY NON-EXISTANT TIME-OUT.
2068	013162	000002				RTI			;RETURN TO MAINSTREAM
2069									
2070	013164	000001				WHICH:	1		
2071	013166	000002					.BYTE	2,2	
2072	013170	001306					STMP4		
2073									
2074	013172	032737	000001	001446		VECMAP:	BIT	#SW00,STRTSW	
2075	013200	001114					BNE	5S	
2076	013202	012737	000340	000022			MOV	#340,2#22	;SET IOT TRAP PRIO TO 7
2077	013210	012737	013364	000020			MOV	#4S,2#20	;SET IOT TRAP VECTOR
2078	013216	012702	002100				MOV	#KM.MAP,R2	;SET SOFTWARE POINTER
2079	013222	012700	000300				MOV	#300,R0	;FLOATING VECTORS START HERE.
2080	013226	012701	000302				MOV	#302,R1	;PC OF IOT INSTR.
2081	013232	010120			1S:		MOV	R1,(R0)+	;START FILLING VECTOR AREA
2082	013234	012721	000004				MOV	#4,(R1)+	;WITH .+2; IOT
2083	013240	022021					CMP	(R0)+(R1)+	;ADD 2 TO R0 +R1
2084	013242	020127	001000				CMP	R1,#1000	
2085	013246	101771					BLOS	1S	;BR IF MORE TO FILL
2086	013250	013737	001470	001276			MOV	KMACTV,STMP0	;STORE TEMPORALLY
2087	013256	006037	001276		2S:		ROR	STMP0	;BRING OUT A BIT
2088	013262	103063					BCC	5S	;BR IF ALL DONE
2089	013264	012704	000012				MOV	#12,R4	;R4 IS INDEX REGISTER
2090	013270	016437	013442	177776			MOV	BRLVL(R4),PS	;SET PS TO 7
2091	013276	011201					MOV	(R2),R1	
2092	013300	012761	000200	000004			MOV	#200,4(R1)	
2093	013306	012711	001000				MOV	#BIT9,(R1)	;SET ROMI
2094	013312	012761	121111	000006			MOV	#121111,6(R1)	;PUT INSTRUCTION IN PORT6
2095	013320	012711	001400				MOV	#BIT9!BIT8,(R1)	;FORCE AN INTERRUPT
2096	013324	105200			7S:		INCB	R0	;STALL
2097	013326	001376					BNE	.-2	;FOR TIME TO INTERRUPT
2098	013330	162704	000002				SUB	#2,R4	;GET NEXT LOWEST PS LEVEL
2099	013334	001404					BEQ	6S	;BR IF R4 = 0
2100	013336	016437	013442	177776			MOV	BRLVL(R4),PS	;MOVE NEXT LOWER LEVEL IN PS
2101	013344	000767					BR	7S	;BR TO DELAY
2102	013346	052762	005300	000002	6S:		BIS	#5300,2(R2)	;NO INTERRUPT ASSUME 300 AT LEVEL 5 AND FIX KMC11 LATER
2103	013354	005011			3S:		CLR	(R1)	;CLEAR ROMI
2104	013356	062702	000010				ADD	#10,R2	;POP SOFTWARE POINTER
2105	013362	000735					BR	2S	;KEEP GOING
2106	013374	051662	000002		4S:		BIS	(SP),2(R2)	;GET VECTOR ADDRESS
2107	013370	042762	000007	000002			BIC	#7,2(R2)	;CLEAR JUNK
2108	013376	016405	013444				MOV	BRLVL+2(R4),R5	;GET BR LEVEL OF KMC11
2109	013402	006305					ASL	R5	;SHIFT LEVEL 4 PLACES
2110	013404	006305					ASL	R5	;TO THE LEFT FOR THE
2111	013406	006305					ASL	R5	;STATUS TABLE
2112	013410	006305					ASL	R5	
2113	013412	042705	170777				BIC	#170777,R5	;CLEAR UNWANTED BITS
2114	013416	050562	000002				BIS	R5,2(R2)	;PUT BR LEVEL IN STATUS TABLE
2115	013422	022626					CMP	(SP)+(SP)+	;POP IOT JUNK OFF STACK
2116	013424	012716	013354				MOV	#3S,(SP)	;SET FOR RETURN
2117	013430	000002					RTI		
2118	013432	012737	004134	000020	5S:		MOV	#SCOPE,2#20	;RESTORE SCOPE VECTOR
2119	013440	000207					RTS	PC	;ALL DONE WITH "AUTO SIZING"
2120									
2121	013442	000000				BRLVL:	PRO	;LEVEL 0	

2122	013444	000000		PRO	:LEVEL 0	
2123	013446	000200		PR4	:LEVEL 4	
2124	013450	000240		PR5	:LEVEL 5	
2125	013452	000300		PR6	:LEVEL 6	
2126	013454	000340		PR7	:LEVEL 7	
2127						
2128						
2129	013456	105777	165562	INTTY: TSTB	2STKS	;WAIT FOR DONE
2130	013462	100375		BPL	.-4	
2131	013464	017703	165556	MOV	2STKB,R3	;PUT CHAR IN R3
2132	013470	105777	165554	TSTB	2STPS	;WAIT UNTIL PRINTER IS READY
2133	013474	100375		BPL	.-4	
2134	013476	010377	165550	MOV	R3,2STPB	;ECHO CHAR
2135	013502	042703	000240	BIC	#BIT7:BIT5,R3	;MASK OFF LOWER CASE
2136	013506	000207		RTS	PC	;RETURN
2137						
2138	013510			APT.SIZE:		
2139	013510	000005		RESET		
2140	013512	010046		MOV	R0,-(SP)	;PUSH R0 ON STACK
2141	013514	010146		MOV	R1,-(SP)	;PUSH R1 ON STACK
2142	013516	010246		MOV	R2,-(SP)	;PUSH R2 ON STACK
2143	013520	010346		MOV	R3,-(SP)	;PUSH R3 ON STACK
2144	013522	005037	013724	CLR	VECTR	CLEAR THE LOCAL VARIABLE
2145	013526	005037	013730	CLR	PRTY	CLEAN UP LOCAL VARIABLE
2146	013532	013700	001376	MOV	\$CDW1,R0	GET THE DEVICE COUNT
2147	013536	010037	001476	MOV	R0,SAVNUM	SAVE THE NO. OF DEVICES
2148	013542	012701	001346	MOV	#1,SI,R1	GET EXTRA INFO. BITS POINTER
2149	013546	013737	001372	MOV	\$BASE,BASE	GET BASE CSR ADDRESS
2150	013554	113737	001366	MOVB	\$VECT1,VECTR	GET THE VECTOR
2151	013562	113737	001357	MOVB	\$VECT1+1,PRTY	GET THE PRIORITY
2152	013570	013737	001374	MOV	\$KACTV,KMACTV	SAVE THE KMC'S SELECTED ACTIVE
2153	013576	013737	001470	MOV	KMACTV,SAVACT	SAVE THE ACTIVE REGISTER
2154	013604	012702	001402	MOV	#DDW0,R2	GET ADDRESS OF FIRST DEVICE DESCRIPTOR WORD
2155	013610	012703	002100	MOV	#KM.MAP,R3	GET POINTER TO DEVICE MAP
2156	013614	005023		3\$: CLR	(R3)+	CLEAR DEVICE MAP
2157	013616	002703	002300	CMP	#KM.END,R3	IS WHOLE DEV MAP CLEARED?
2158	013622	003374		BGT	3\$	NO, THEN GO ON.
2159	013624	012703	002100	MOV	#KM.MAP,R3	RESTORE DEV.MAP POINTER.
2160	013630	013723	013726	1\$: MOV	BASE,(R3)+	LOAD CSR ADDRESS
2161	013634	112163	000001	MOVB	(R1)+,1(R3)	GET EXTRA INFO. BITS
2162	013640	006213		ASR	(R3)	SET IT IN RIGHT POSITION.
2163	013642	006213		ASR	(R3)	SET IT IN RIGHT POSITION.
2164	013644	053713	013730	BIS	PRTY,(R3)	GET PRIORITY IN STAT1
2165	013650	006313		ASL	(R3)	SET THEM IN RIGHT POSITION
2166	013652	006313		ASL	(R3)	" " " " " "
2167	013654	006313		ASL	(R3)	" " " " " "
2168	013656	006313		ASL	(R3)	" " " " " "
2169	013660	053723	013724	BIS	VECTR,(R3)+	GET THE VECTOR IN STAT1.
2170	013664	012223		MOV	(R2)+,(R3)+	GET THE STAT2 FROM DDWXX
2171	013666	005723		TST	(R3)+	SKIP OVER STAT3
2172	013670	005300		DEC	R0	COUNT BY 1
2173	013672	001407		BEQ	2\$	ALL DONE?
2174	013674	062737	000010	ADD	#10,BASE	INCREMENT BASE CSR ADDRESS BY 10
2175	013702	062737	000010	ADD	#10,VECTR	INCREMENT VECTOR ADDRESS BY 10
2176	013710	000747		BR	1\$	SET THE NEXT MAP ENTRY
2177	013712			2\$:		



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 DZKCD.P11 21-MAY-77 17:24 POWER DOWN AND UP ROUTINES

PAGE: 0064

2178	013712	012603	MOV	(SP)+,R3	::POP STACK INTO R3
2179	013714	012602	MOV	(SP)+,R2	::POP STACK INTO R2
2180	013716	012601	MOV	(SP)+,R1	::POP STACK INTO R1
2181	013720	012600	MOV	(SP)+,R0	::POP STACK INTO R0
2182	013722	000207	RTS	PC	::RETURN
2183	013724	000000	VECTR:	.WORD 0	
2184	013726	000000	BASE:	.WORD 0	
2185	013730	000000	PRIPTY:	.WORD 0	
2186					
2187	013732		ROMMAP:		

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\*\*\*\*\* TEST 1 \*\*\*\*\*  
\*TEST OF BR RIGHT SHIFT  
\*VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION  
\*SHIFTS THE RESULTING BR DATA RIGHT ONCE.  
\*\*\*\*\*

TEST 1

\*\*\*\*\*

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†ST1: SCOPE
MOV #1,$STNM ; LOAD THE NO. OF THIS TEST
MOV #TST2,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
MOV KMCSR,R1 ; R1 = KMC BASE ADDRESS
CLR (R1) ; CLEAR SELD
MOV #52525,R5 ; START WITH 125
MOV R5,4(R1) ; PORT4+125
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
120500 ; BR + PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
061620 ; BR RSH+BR, SHIFT BR RIGHT
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
061225 ; PORT5+BR
ROR R5 ; R5 = "EXPECTED"
MOVB 5(R1),R4 ; R4 = "FOUND"
CMPB R5,R4 ; DID BR SHIFT RIGHT ONCE?
REQ 1$ ; BR IF YES
ERROR 12 ; BR RIGHT SHIFT ERROR

1$: ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
061620 ; BR RSH+BR, SHIF BR RIGHT AGAIN
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
061225 ; PORT5+BR
ROR R5 ; R5 = "EXPECTED"
MOVB 5(R1),R4 ; R4 = "FOUND"
CMPB R5,R4 ; DID BR SHIFT RIGHT?
REQ 2$ ; BR IF YES
ERROR 12 ; BR RIGHT SHIFT ERROR

2$:

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\*\*\*\*\* TEST 2 \*\*\*\*\*  
\*IOP CRAM WRITE/READ TEST  
\*FLOAT A 1 THROUGH EACH CRAM LOCATION  
\*\*\*\*\*

TEST 2

\*\*\*\*\*

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†ST2: SCOPE
MOV #2,$STNM ; LOAD THE NO. OF THIS TEST
MOV #TST3,NEXT ; POINT TO THE START OF NEXT TEST.

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2244 014062 012737 014076 001444      MOV      #3$,LOCK      ; ADDRESS FOR LOCK ON DATA.
2245                                ; R1 CONTAINS BASE KMC11 ADDRESS
2246 014070 005000      CLR      R0            ; R0 = CRAM ADDRESS
2247 014072 012702 000001      1$: MOV      #1,R2      ; R2 = WRITE DATA
2248 014076                                ;
2249 014076 012711 002000      2$: MOV      #BIT10,(R1) ; SET ROMO
2250 014102 010061 000004      3$: MOV      R0,4(R1)   ; WRITE ADDRESS TO SEL4
2251 014106 010261 000006      MOV      R2,6(R1)   ; LOAD SEL6 WITH WRITE DATA
2252 014112 052711 020000      BIS      #BIT13,(R1) ; WRITE SEL6 INTO CRAM
2253 014116 016104 000004      MOV      4(R1),R4   ; READ CRAM INTO "FOUND"
2254 014122 020204      CMP      R2,R4      ; IS DATA CORRECT?
2255 014124 001401      BEQ     4$          ; BR IF OK
2256 014126 104001      ERROR   1          ; ERROR
2257 014130 104405      4$: SCOPI
2258 014132 000241      CLC
2259 014134 006102      ROL     R2          ; CLEAR CARRY
2260 014136 001357      BNE     2$          ; SHIFT WRITE DATA
2261 014140 005200      INC     R0          ; BR IF NOT DONE THIS ADDRESS
2262 014142 022700 002000      CMP     #2000,R0   ; BUMP TO NEXT CRAM ADDRESS
2263 014146 001351      BNE     1$          ; DONE YET?
2264 014150      5$: BR     IF NO
2265
2266
2267      ;***** TEST 3 *****
2268      ;IOP CRAM WRITE/READ TEST
2269      ;FLOAT A 0 THROUGH EACH CRAM LOCAT:ON
2270      ;*****
2271
2272      ; TEST 3
2273      ;-----
2274      ;*****
2275 014150 000004      1$: SCOPE
2276 014152 012737 000003 001202      MOV     #3,$STSTM   ; LOAD THE NO. OF THIS TEST
2277 014160 012737 014262 001442      MOV     #TST4,NEXT ; POINT TO THE START OF NEXT TEST.
2278 014166 012737 014206 001444      MOV     #3$,LOCK   ; ADDRESS FOR LOCK ON DATA.
2279                                ; R1 CONTAINS BASE KMC11 ADDRESS
2280 014174 104410      MSTCLR ; MASTER CLEAR KMC11
2281 014176 005000      CLR     R0          ; R0 = CRAM ADDRESS
2282 014200 012702 000001      1$: MOV     #1,R2    ; R2 = WRITE DATA
2283 014204                                ;
2284 014204 005102      2$: COM     R2      ; MAKE IT A FLOATING ZERO
2285 014206 012711 002000      3$: MOV     #BIT10,(R1) ; SET ROMO
2286 014212 010061 000004      MOV     R0,4(R1)   ; WRITE ADDRESS TO SEL4
2287 014216 010261 000006      MOV     R2,6(R1)   ; LOAD SEL6 WITH WRITE DATA
2288 014222 052711 020000      BIS     #BIT13,(R1) ; WRITE SEL6 INTO CRAM
2289 014226 016104 000004      MOV     4(R1),R4   ; READ CRAM INTO "FOUND"
2290 014232 020204      CMP     R2,R4      ; IS DATA CORRECT?
2291 014234 001401      BEQ    4$          ; BR IF OK
2292 014236 104001      ERROR   1          ; ERROR
2293 014240 104405      4$: SCOPI
2294 014242 005102      COM     R2          ; BACK TO FLOATING ONE
2295 014244 000241      CLC
2296 014246 006102      ROL     R2          ; CLEAR CARRY
2297 014250 001355      BNE     2$          ; SHIFT WRITE DATA
2298 014252 005200      INC     R0          ; BR IF NOT DONE THIS ADDRESS
2299 014254 022700 002000      CMP     #2000,R0   ; BUMP TO NEXT CRAM ADDRESS
                                ; DONE YET?

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2300 014260 001347
2301 014262
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2313 014262 000004
2314 014264 012737 000004 001202
2315 014272 012737 014432 001442
2316 014300 012737 014312 001444
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2318 014306 104410
2319 014310 005000
2320 014312 010002
2321 014314 012711 002000
2322 014320 010061 000004
2323 014324 010061 000006
2324 014330 012711 020000
2325 014334 005061 000006
2326 014340 016104 000006
2327 014344 020004
2328 014346 001401
2329 014350 104001
2330 014352 104405
2331 014354 005200
2332 014356 022700 002000
2333 014362 001353
2334 014364 005000
2335 014366 012737 014374 001444
2336 014374 010002
2337 014376 012711 002000
2338 014402 010061 000004
2339 014406 016104 000006
2340 014412 020004
2341 014414 001401
2342 014416 104002
2343 014420 104405
2344 014422 005200
2345 014424 022700 002000
2346 014430 001361
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5$: BNE 1$ ;BR IF NO
5$:
:***** TEST 4 *****
: IOP CROM DUAL ADDRESSING TEST
: WRITE EACH ADDRESS INTO ITSELF, READ EACH
: ADDRESS TO VERIFY CORRECT ADDRESSING
:*****
: TEST 4
:-----
:*****
1$T4: SCOPE
MOV #4, $TSTNM ; LOAD THE NO. OF THIS TEST
MOV #TSTS, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$, LOCK ; ADDRESS FOR LOCK ON DATA.
: R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR RO ; RO = CROM ADDRESS
1$: MOV RO, R2 ; SAVE R2 FOR TYPEOUT
MOV #BIT10, (R1) ; SET ROMO
MOV RO, 4(R1) ; WRITE ADDRESS TO SEL4
MOV RO, 6(R1) ; LOAD SEL6 WITH WRITE DATA
BIS #BIT13, (R1) ; WRITE CROM
CLR 6(R1) ; CLEAR SEL 6
MOV 6(R1), R4 ; SHOULD READ BACK OWN ADDRESS
CMP RO, R4 ; IS DATA CORRECT?
BEQ 2$ ; BR IF YES
ERROR 1 ; DATA ERROR
2$: SCOP1 ; LOOP TO 1$ IF SW09=1
INC RO ; BUMP TO NEXT ADDRESS
CMP #2000, RO ; DONE WRITING YET?
BNE 1$ ; BR IF NO
CLR RO ; RESTART AT ADDRESS 0
MOV #3$, LOCK ; NEW SCOP1
3$: MOV RO, R2 ; SAVE R2 FOR TYPEOUT
MOV #BIT10, (R1) ; SET ROMO
MOV RO, 4(R1) ; SEL4 = CROM ADDRESS
MOV 6(R1), R4 ; READ CROM INTO "FOUND"
CMP RO, R4 ; IS DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 2 ; DUAL ADDRESSING ERROR
4$: SCOP1 ; LOOP TO 3$ IF SW09=1
INC RO ; BUMP TO NEXT ADDRESS
CMP #2000, RO ; DONE WRITING YET?
BNE 3$ ; BR IF NO
5$:
:***** TEST 5 *****
: IOP CROM READ TEST
: THIS TEST WRITES THE CROM WITH THE CROM MICRO-CODE MAP
: THEN READS IT BACK AND COMPARES EACH ADDRESS WITH THE
: DUPLICATE OF THE CROM MICRO-CODE.
:*****

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2360 014432 000004
2361 014434 012737 000005 001202
2362 014442 012737 014542 001442
2363 014450 012737 014474 001444
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2365 014456 104410
2366 014460 005011
2367 014462 004737 021140
2368 014466 012700 013732
2369 014472 005002
2370 014474 010261 000004
2371 014500 012711 002000
2372 014504 011005
2373 014506 016104 000006
2374 014512 J20504
2375 014514 001401
2376 014516 104003
2377 014520 005011
2378 014522 005061 000006
2379 014526 104405
2380 014530 005202
2381 014532 005720
2382 014534 022702 002000
2383 014540 001355
2384 014542

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; TEST 5
;-----
;*****
TSTS: SCOPE
MOV #5, $TSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST6, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$, LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR (R1) ; CLEAR RUN
JSR PC, WROM ; WRITE CROM WITH MAP
MOV #ROMMAP, R0 ; SOFTWARE POINTER TO CROM DUPLICATE
CLR R2 ; R2 = CROM ADDRESS
1$: MOV R2, 4(R1) ; WRITE CROM ADDRESS TO SEL4
MOV #BIT10, (R1) ; SET CROM0
MOV (R0), R5 ; PUT "EXPECTED" IN R5
MOV 5(R1), R4 ; PUT "FOUND" IN R4
CMP R5, R4 ; COMPARE HARD ROM TO SOFT DUPLICATE
BEQ 2$ ; BR IF OK
ERROR 3 ; CROM READ ERROR!
2$: CLR (R1) ; CLR BIT10
CLR 6(R1) ; CLEAR SEL6
SCOPI ; LOOP TO 1$ IF SW09=1
INC R2 ; INC TO NEXT CROM ADDRESS
TST (R0)+ ; POP R0 BY 2
CMP #2000, R2 ; DONE 1K YET?
BNE 1$ ; BR IF NO
3$:

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2395 014542 000004
2396 014544 012737 000006 001202
2397 014552 012737 014720 001442
2398 014560 012737 014600 001444
2399
2400 014566 104410
2401 014570 005037 021012
2402 014574 012700 000001
2403 014600 042737 000377 014632
2404 014606 042737 000003 014636
2405 014614 153737 021012 014632
2406 014622 153737 021013 014636
2407 014630 104412
2408 014632 010000
2409 014634 104412
2410 014636 004000
2411 014640 010061 000004

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;***** TEST 6 *****
;IOP MAIN MEMORY TEST
;FLOAT A 1 THROUGH ALL MAIN MEMORY LOCATIONS
;*****
; TEST 6
;-----
;*****
TST6: SCOPE
MOV #6, $TSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST7, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #65$, LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR FLAG ; START WITH ADDRESS 0
1$: MOV #1, R0 ; START WITH BIT 0
65$: BIC #377, 66$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIC #3, 68$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BISB FLAG, 66$ ; ADD ADDRESS TO INSTRUCTION
BISB FLAG+1, 68$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR LO WITH ADDRESS IN FLAG
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
004000 ; LOAD MAR HI
68$: MOV R0, 4(R1) ; WRITE PATTERN IN PORT4

```



2468 015050 001401  
 2469 015052 104010  
 2470 015054 104405  
 2471 015056 005100  
 2472 015060 000241  
 2473 015062 106100  
 2474 015064 001334  
 2475 015066 005237 021012  
 2476 015072 022737 002000 021012  
 2477 015100 001324  
 2478 015102

67\$: BEQ 67\$  
 ERROR 10  
 SCOPE1  
 COM R0  
 CLC  
 ROLB R0  
 BNE 64\$  
 INC FLAG  
 CMP #2000,FLAG  
 BNE 1\$

2\$:

: BR IF YES  
 : DATA ERROR  
 : SW09=1?  
 : CHANGE TO FLOATING 1  
 : CLEAR CARRY  
 : SHIFT BIT IN R0  
 : DONE IF R0=0  
 : NEXT ADDRESS  
 : LAST ADDRESS?  
 : BR IF NO

:\*\*\*\*\* TEST 10 \*\*\*\*\*  
 : IOP MAIN MEMORY DUAL ADDRESSING TEST  
 : LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS  
 : READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING  
 :\*\*\*\*\*

TEST 10

2481  
 2482  
 2483  
 2484  
 2485  
 2486  
 2487  
 2488  
 2489  
 2490 015102 000004  
 2491 015104 012737 000010 001202  
 2492 015112 012737 015372 001442  
 2493 015120 012737 015134 001444  
 2494  
 2495  
 2496 015126 104410  
 2497 015130 005037 021012  
 2498 015134 013702 021012  
 2499 015140 042737 000377 015172  
 2500 015146 042737 000003 015176  
 2501 015154 153737 021012 015172  
 2502 015162 153737 021013 015176  
 2503 015170 104412  
 2504 015172 010000  
 2505 015174 104412  
 2506 015176 004000  
 2507 015200 010261 000004  
 2508 015204 104412  
 2509 015206 122500  
 2510 015210 104412  
 2511 015212 040620  
 2512 015214 104412  
 2513 015216 061225  
 2514 015220 010205  
 2515 015222 116104 000005  
 2516 015226 120504  
 2517 015230 001401  
 2518 015232 104010  
 2519 015234 104405  
 2520 015236 005237 021012  
 2521 015242 022737 002000 021012  
 2522 015250 001331  
 2523 015252 012737 015264 001444  
 2524 015260 005037 021012

1\$: MSTCLR  
 CLR FLAG  
 MOV FLAG,R2  
 BIC #377,2\$  
 BIC #3,7\$  
 BISB FLAG,2\$  
 BISB FLAG+1,7\$  
 ROMCLK  
 010000  
 ROMCLK  
 004000  
 MOV R2,4(R1)  
 ROMCLK  
 122500  
 ROMCLK  
 040620  
 ROMCLK  
 61225  
 MOV R2,R5  
 ST(R1),R4  
 MOV R3,R4  
 CMP R3,R4  
 BEQ 3\$  
 ERROR 10  
 SCOPE1  
 INC FLAG  
 CMP #2000,FLAG  
 BNE 1\$  
 MOV #4\$,LOCK  
 CLR FLAG

2\$: 010000  
 7\$: 004000  
 3\$:

:\*\*\*\*\*  
 : LOAD THE NO. OF THIS TEST  
 : POINT TO THE START OF NEXT TEST.  
 : ADDRESS FOR LOCK ON DATA.  
 : R1 CONTAINS BASE KMC11 ADDRESS  
 : MASTER CLEAR KMC11  
 : START AT ADDRESS 0  
 : PUT DATA IN R2  
 : CLEAR ADDRESS FIELD OF INSTRUCTION  
 : CLEAR ADDRESS FIELD OF INSTRUCTION  
 : ADD ADDRESS TO INSTRUCTION  
 : ADD ADDRESS TO INSTRUCTION  
 : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 : LOAD MAR LO  
 : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 : LOAD MAR HI  
 : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 : MOVE PORT4 TO MEMORY  
 : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 : MOVE MEMORY TO THE BR  
 : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 : MOV BR TO PORTS  
 : PUT "EXPECTED" IN R5  
 : PUT "FOUND" IN R4  
 : DATA CORRECT?  
 : BR IF YES  
 : DATA ERROR  
 : SW09=1?  
 : NEXT ADDRESS  
 : LAST ADDRESS  
 : BR IF NO  
 : NEW SCOPE 1  
 : RESTART AT ADDRESS 0

2524	015264	013702	021012		45:	MOV	FLAG,R2	; PUT DATA IN R2
2525	015270	042737	000377	015322		BIC	#377,5\$	; CLEAR ADDRESS FIELD OF INSTRUCTION
2526	015276	042737	000003	015326		BIC	#3,8\$	; CLEAR ADDRESS FIELD OF INSTRUCTION
2527	015304	153737	021012	015322		BISB	FLAG,5\$	; ADD ADDRESS TO INSTRUCTION
2528	015312	153737	021013	015326		BISB	FLAG+1,8\$	; ADD ADDRESS TO INSTRUCTION
2529	015320	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2530	015322	010000			55:	010000		; LOAD THE MAR LO
2531	015324	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2532	015326	004000			85:	004000		; LOAD MAR HI
2533	015330	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2534	015332	040620				040620		; MOVE MEMORY TO THE BR
2535	015334	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2536	015336	061225				61225		; MOV BR TO PORTS
2537	015340	010205				MOV	R2,R5	; PUT "EXPECTED" IN R5
2538	015342	116104	000005			MOVB	5(R1),R4	; PUT "FOUND" IN R4
2539	015346	120504				CMPB	R5,R4	; DATA CORRECT?
2540	015350	001401				BEQ	6\$	; BR IF YES
2541	015352	104010				ERROR	10	; ADDRESSING ERROR
2542	015354	104405			65:	SCOPI		; SW09=1?
2543	015356	005237	021012			INC	FLAG	; NEXT ADDRESS
2544	015362	022737	002000	021012		CMP	#2000,FLAG	; IS IT THE LAST
2545	015370	001335				BNE	4\$	; BR IF NO
2546	015372				95:			

```

:***** TEST 11 *****
: *IOP MAR TEST
: *PERFORM DUAL ADDRESSING TEST
: *USING MAR AUTO-INC FEATURE
:*****

```

TEST 11

2557								
2558	015372	000004			15:	SCOPE		;*****
2559	015374	012737	000011	001202	TST11:	MOV	#11,\$STNM	; LOAD THE NO. OF THIS TEST
2560	015402	012737	015476	001442		MOV	#TST12,NEXT	; POINT TO THE START OF NEXT TEST.
2561								; R1 CONTAINS BASE KMC11 ADDRESS
2562	015410	104410				MSTCLR		; MASTER CLEAR KMC11
2563	015412	005002				CLR	R2	; START WITH A ZERO
2564	015414	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2565	015416	010000				010000		; LOAD MAR WITH A ZERO
2566	015420	010261	000004		15:	MOV	R2,4(R1)	; WRITE DATA TO PORT4
2567	015424	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2568	015426	136500				136500		; MEM+PORT4, AUTO-INC MAR
2569	015430	005202				INC	R2	; INCREMENT DATA
2570	015432	022702	002000			CMP	#2000,R2	; DONE YET?
2571	015436	001370				BNE	1\$	; BR IF NO
2572	015440	005002				CLR	R2	; RESTART WITH A ZERO
2573	015442	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2574	015444	010000				010000		; LOAD MAR WITH A ZERO
2575	015446				25:			
2576	015446	104412				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2577	015450	055224				055224		; MOVE MEM TO PORT4
2578	015452	010205				MOV	R2,R5	; PUT "EXPECTED" IN R5
2579	015454	016104	000004			MOV	4(R1),R4	; PUT "FOUND" IN R4



2580 015460 120504  
 2581 015462 001401  
 2582 015464 104011  
 2583 015466 005202  
 2584 015470 022702 002000  
 2585 015474 001364  
 2586 015476

3\$: CMPB R5,R4 ; DATA CORRECT?  
 BEQ 3\$ ; BR IF YES  
 ERROR 11 ; MAR ERROR  
 4\$: INC R2 ; NEXT ADDRESS  
 CMP #2000,R2 ; DONE YET?  
 BNE 2\$ ; BR IF NO

\*\*\*\*\* TEST 12 \*\*\*\*\*  
 ; IOP (GRAM) OOT BITS TEST  
 ; LOAD MAR WITH A 0 INC MAR UNTIL IT OVERFLOWS (2000 TIMES)  
 ; VERIFY THAT IBUS\* 10 BITS IS SET ONLY WHEN MAR BIT 8 IS A ONE  
 ; AND THAT IBUS\* 10 BIT6 IS SET ON MAR OVERFLOW(2000)  
 ; \*\*\*\*\*

TEST 12

2599 015476 000004  
 2600 015500 012737 000012 001202  
 2601 015506 012737 015674 001442  
 2602 015514 012737 015532 001444  
 2603  
 2604 015522 104410  
 2605 015524 005002  
 2606 015526 104412  
 2607 015530 010000  
 2608 015532  
 2609 015532 104412  
 2610 015534 121204  
 2611 015536 005005  
 2612 015540 032702 000400  
 2613 015544 001402  
 2614 015546 012705 000040  
 2615 015552 016104 000004  
 2616 015556 042704 177637  
 2617 015562 020504  
 2618 015564 001401  
 2619 015566 104007  
 2620 015570 104405  
 2621 015572 104412  
 2622 015574 014000  
 2623 015576 005202  
 2624 015600 022702 002000  
 2625 015604 001352  
 2626 015606 005037 001444  
 2627 015612 104412  
 2628 015614 121204  
 2629 015616 012705 000100  
 2630 015622 016104 000004  
 2631 015626 042704 177637  
 2632 015632 020504  
 2633 015634 001401  
 2634 015636 104007  
 2635 015640 104412

1\$: \*\*\*\*\*  
 TST12: SCOPE ; LOAD THE NO. OF THIS TEST  
 MOV #12,\$TSTNM ; POINT TO THE START OF NEXT TEST.  
 MOV #TST13,NEXT ; ADDRESS FOR LOCK ON DATA.  
 MOV #1\$,LOCK ; R1 CONTAINS BASE KMC11 ADDRESS  
 ; MASTER CLEAR KMC11  
 MSTCLR ; R2= SAME AS MAR CONTENTS  
 CLR R2 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 ROMCLK ; MAR=0  
 010000 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 121204 ; PART4=IBUS\* 10  
 CLR R5 ; R5="EXPECTED"  
 BIT #BIT8,R2 ; IS BIT8 SET IN MAR?  
 BEQ .+6 ; BR IF NO  
 MOV #BIT5,R5 ; IF YES THEN SET BITS  
 MOV 4(R1),R4 ; R4="FOUND"  
 BIC #177637,R4 ; CLEAR UNWANTED BITS  
 CMP R5,R4 ; BITS 5&6 SHOULD BE CLEAR  
 BEQ .+4 ; BR IF OK  
 ERROR 7 ; ERROR BITS 5&6 NOT CLEAR  
 SCOPI ; LOOP TO 11\$ IF SW09=1  
 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 014000 ; INC MAR  
 INC R2 ; BUMP MEM ADDRESS  
 CMP #2000,R2 ; OVERFLOWED YET?  
 BNE 1\$ ; BR IF NO  
 CLR LOCK ; NO MORE SCOPI  
 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
 121204 ; PART4=IBUS\* 10  
 MOV #BIT6,R5 ; R5="EXPECTED"  
 MOV 4(R1),R4 ; R4="FOUND"  
 BIC #177637,R4 ; CLEAR UNWANTED BITS  
 CMP R5,R4 ; BIT6 SHOULD BE SET  
 BEQ .+4 ; BR IF OK  
 ERROR 7 ; ERROR, BIT6 NOT SET  
 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

2636	015642	010000		010000					;MAR←0
2637	015644	104412		ROMCLK					;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2638	015646	004000		004000					;MAR HI←0
2639	015650	104412		ROMCLK					;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2640	015652	121204		121204					;PORT4←IBUS* 10
2641	015654	005005		CLR	R5				;R5="EXPECTED"
2642	015656	016104	000004	MOV	4(R1),R4				;R4="FOUND"
2643	015662	042704	177637	BIC	#177637,R4				;CLEAR UNWANTED BITS
2644	015666	020504		CMP	R5,R4				;BITS 5&6 SHOULD BE CLEAR
2645	015670	001401		BEQ	+4				;BR IF OK
2646	015672	104007		ERROR	7				;ERROR 5&6 NOT BOTH CLEAR
2647	015674								

2\$:

```

***** TEST 13 *****
*CRAM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.
*PERFORM THE JUMP INSTRUCTION
*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT, THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
*THEN PORT4 CONTAINS A 37
:*****

```

TEST 13

2661									
2662									
2663									
2664	015674	000004		ST13: SCOPE					
2665	015676	012737	000013	MOV	#13,\$STSTNM				; LOAD THE NO. OF THIS TEST
2666	015704	012737	016060	MOV	#TST14,NEXT				; POINT TO THE START OF NEXT TEST.
2667	015712	012737	015726	MOV	#1\$,LOCK				; ADDRESS FOR LOCK ON DATA.
2668									;R1 CONTAINS BASE KMC11 ADDRESS
2669	015720	104410		MSTCLR					;MASTER CLEAR KMC11
2670	015722	004737	021202	JSR	PC, MEMSET				;SET MEM AND RAM
2671	015726								
2672	015726	004737	021014	JSR	PC, CLRALL				;CLEAR ALL CONDITIONS
2673	015732	104412		ROMCLK					;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2674	015734	100400		100400					;START AT ROM PC=0
2675	015736	104412		ROMCLK					;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2676	015740	114377		114377!<400*0>					;JUMP TO ROM PC OF 1777
2677	015742	004737	021106	JSR	PC, RAMDAT				;R4=CRAM PC (LSB 8 BITS)
2678	015746	000001		1					;EXPECTED DATA
2679	015750	120504		CMPB	R5,R4				;IS ROM PC CORRECT?
2680	015752	001401		BEQ	2\$				;BR IF YES
2681	015754	104005		ERROR	5				;ERROR, CRAM PC IS WRONG
2682	015756	104405		SCOPI					;LOOP TO 1\$ IF SW09=1
2683	015760	012737	015766	MOV	#3\$,LOCK				;NEW SCOPI
2684	015766								
2685	015766	004737	021014	JSR	PC, CLRALL				;CLEAR ALL CONDITIONS
2686	015772	104412		ROMCLK					;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2687	015774	100403		100403					;START AT ROM PC=3
2688	015776	104412		ROMCLK					;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2689	016000	100000		100000!<400*0>					;JUMP TO ROM PC OF 0
2690	016002	004737	021106	JSR	PC, RAMDAT				;R4=CRAM PC (LSB 8 BITS)
2691	016006	000004		4					;EXPECTED DATA

1\$:

2\$:

3\$:

```

2692 016010 120504          CMPB   R5,R4          ; IS ROM PC CORRECT?
2693 016012 001401          BEQ    4$             ; BR IF YES
2694 016014 104005          ERROR  5             ; ERROR, CRAM PC IS WRONG
2695 016016 104405          SCOPI                     ; LOOP TO 3$ IF SW09=1
2696 016020 012737 016026 001444 4$:  MOV    #5$,LOCK      ; NEW SCOPI
2697 016026          5$:
2698 016026 004737 021014      JSR    PC,CLRALL      ; CLEAR ALL CONDITIONS
2699 016032 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2700 016034 100406          100406  ; START AT ROM PC=6
2701 016036 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2702 016040 104125          104125!<400*0>      ; JUMP TO ROM PC OF 525
2703 016042 004737 021106      JSR    PC,RAMDAT      ; R4=CRAM PC (LSB 8 BITS)
2704 016046 000007          7             ; EXPECTED DATA
2705 016050 120504          CMPB   R5,R4          ; IS ROM PC CORRECT?
2706 016052 001401          BEQ    6$             ; BR IF YES
2707 016054 104005          ERROR  5             ; ERROR, CRAM PC IS WRONG
2708 016056 104405          SCOPI                     ; LOOP TO 5$ IF SW59=1
2709
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2721
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2724

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```

***** TEST 14 *****
; *CRAM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.
; *PERFORM THE JUMP INSTRUCTION
; *VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
; *IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
; *BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
; *THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
; *THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
; *THEN PORT4 WILL CONTAIN A 37
; *****

```

TEST 14

```

2725 016060 000004          1$T14: SCOPE
2726 016062 012737 000014 001202  MOV    #14,$ISTIM     ; LOAD THE NO. OF THIS TEST
2727 016070 012737 016230 001442  MOV    #1$T15,NEXT    ; POINT TO THE START OF NEXT TEST.
2728 016076 012737 016112 001444  MOV    #1$,LOCK       ; ADDRESS FOR LOCK ON DATA.
2729
2730 016104 104410          MSTCLR  ; R1 CONTAINS BASE KMC11 ADDRESS
2731 016106 004737 021202      JSR    PC,MEMSET      ; MASTER CLEAR KMC11
2732 016112          1$:
2733 016112 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2734 016114 100400          100400  ; START AT ROM PC=0
2735 016116 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2736 016120 114777          114777!<400*1>      ; JUMP TO ROM PC OF 1777
2737 016122 004737 021106      JSR    PC,RAMDAT      ; R4=CRAM PC (LSB 8 BITS)
2738 016126 000377          377         ; EXPECTED DATA
2739 016130 120504          CMPB   R5,R4          ; IS ROM PC CORRECT?
2740 016132 001401          BEQ    2$             ; BR IF YES
2741 016134 104005          ERROR  5             ; ERROR, CRAM PC IS WRONG
2742 016136 104405          SCOPI                     ; LOOP TO 1$ IF SW09=1
2743 016140 012737 016146 001444 3$:  MOV    #3$,LOCK      ; NEW SCOPI
2744 016146          3$:
2745 016146 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2746 016150 100403          100403  ; START AT ROM PC=3
2747 016152 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

```

2748 016154 100400 100000! <400*1> JUMP TO ROM PC OF 0
2749 016156 004737 021106 JSR PC,RANDAT ;R4=CRAM PC (LSB 8 BITS)
2750 016162 000000 0 ;EXPECTED DATA
2751 016164 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
2752 016166 001401 BEQ 4$ ;BR IF YES
2753 016170 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2754 016172 104405 4$: SCOPI ;LOOP TO 3$ IF SW09=1
2755 016174 012737 016202 001444 MOV #5$,LOCK ;NEW SCOPI
2756 016202 5$:
2757 016202 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2758 016204 100406 100406 ;START AT ROM PC=6
2759 016206 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2760 016210 104525 104125! <400*1> JUMP TO ROM PC OF 525
2761 016212 004737 021106 JSR PC,RANDAT ;R4=CRAM PC (LSB 8 BITS)
2762 016216 000125 125 ;EXPECTED DATA
2763 016220 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
2764 016222 001401 BEQ 6$ ;BR IF YES
2765 016224 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2766 016226 104405 6$: SCOPI ;LOOP TO 5$ IF SW59=1
2767
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2776
2777
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2780
2781
2782

```

```

***** TEST 15 *****
*CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
*SET THE C BIT, PERFORM THE JUMP INSTRUCTION.
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37
*****

```

TEST 15

```

2783 016230 000004 000015 001202 ;*****
2784 016232 012737 000015 001202 †TST15: SCOPE
2785 016240 012737 016414 001442 MOV #15,$STNM ; LOAD THE NO. OF THIS TEST
2786 016246 012737 016262 001444 MOV #TST16,NEXT ; POINT TO THE START OF NEXT TEST.
2787 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
2788 016254 104410 MSTCLR ;R1 CONTAINS BASE KMC11 ADDRESS
2789 016256 004737 021202 JSR PC,MEMSET ;MASTER CLEAR KMC11
2790 016262 15: SET MEM AND RAM
2791 016262 004737 021062 JSR PC,SETC ;SET THE C BIT
2792 016266 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2793 016270 100400 100400 ;START AT ROM PC=0
2794 016272 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2795 016274 115377 114377! <400*2> JUMP TO ROM PC OF 1777
2796 016276 004737 021106 JSR PC,RANDAT ;R4=CRAM PC (LSB 8 BITS)
2797 016302 000377 377 ;EXPECTED DATA
2798 016304 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
2799 016306 001401 BEQ 2$ ;BR IF YES
2800 016310 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2801 016312 104405 2$: SCOPI ;LOOP TO 1$ IF SW09=1
2802 016314 012737 016322 001444 MOV #3$,LOCK ;NEW SCOPI
2803 016322 3$:

```

```

2804 016322 004737 021062 JSR PC,SETC ;SET THE C BIT'
2805 016326 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2806 016330 100403 100403 ;START AT ROM PC=3
2807 016332 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2808 016334 101000 100000!<400*2> JUMP TO ROM PC OF 0
2809 016336 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
2810 016342 000000 0 ;EXPECTED DATA
2811 016344 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
2812 016346 001401 BEQ 4$ ;BR IF YES
2813 016350 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2814 016352 104405 SCOPI ;LOOP TO 3$ IF SW09=1
2815 016354 012737 016362 001444 4$: MOV #5$,LOCK ;NEW SCOPI
2816 016362 5$:
2817 016362 004737 021062 JSR PC,SETC ;SET THE C BIT'
2818 016366 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2819 016370 100406 100406 ;START AT ROM PC=6
2820 016372 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2821 016374 105125 104125!<400*2> JUMP TO ROM PC OF 525
2822 016376 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
2823 016402 000125 125 ;EXPECTED DATA
2824 016404 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
2825 016406 001401 BEQ 6$ ;BR IF YES
2826 016410 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2827 016412 104405 SCOPI ;LOOP TO 5$ IF SW59=1
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***** TEST 16 *****
*CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
*SET THE Z BIT, PERFORM THE JUMP INSTRUCTION,
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37
*****

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; TEST 16

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;*****
;TST16: SCOPE
;MOV #16,$TSTNM ;LOAD THE NO. OF THIS TEST
;MOV #TST17,NEXT ;POINT TO THE START OF NEXT TEST.
;MOV #1$,LOCK ;ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
;MASTER CLEAR KMC11
;SET MEM AND RAM
1$: JSR PC,SETZ ;SET THE Z BIT'
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100400 ;START AT ROM PC=0
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
114377!<400*3> JUMP TO ROM PC OF 1777
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
377 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?

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2844 016414 000004
2845 016416 012737 000016 001202
2846 016424 012737 016600 001442
2847 016432 012737 016446 001444
2848
2849 016440 104410
2850 016442 004737 021202
2851 016446
2852 016446 004737 021100
2853 016452 104412
2854 016454 100400
2855 016456 104412
2856 016460 115777
2857 016462 004737 021106
2858 016466 000377
2859 016470 120504

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2860 016472 001401 BEQ 2$ ;BR IF YES
2861 016474 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2862 016476 104405 2$: SCOPI ;LOOP TO 1$ IF SW09=1
2863 016500 012737 016506 001444 MOV #3$,LOCK ;NEW SCOPI
2864 016506 3$:
2865 016506 004737 021100 JSR PC,SETZ ;SET THE Z BIT'
2866 016512 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2867 016514 100403 100403 ;START AT ROM PC=3
2868 016516 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2869 016520 101400 100000! <400*3> JUMP TO ROM PC OF 0
2870 016522 004737 021105 JSR PC,RANDAT ;R4=CRAM PC (LSB 8 BITS)
2871 016526 000000 0 ;EXPECTED DATA
2872 016530 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
2873 016532 001401 BEQ 4$ ;BR IF YES
2874 016534 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2875 016536 104405 4$: SCOPI ;LOOP TO 3$ IF SW09=1
2876 016540 012737 016546 001444 MOV #5$,LOCK ;NEW SCOPI
2877 016546 5$:
2878 016546 004737 021100 JSR PC,SETZ ;SET THE Z BIT'
2879 016552 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2880 016554 100406 100406 ;START AT ROM PC=6
2881 016556 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2882 016560 105525 104125! <400*3> JUMP TO ROM PC OF 525
2883 016562 004737 021106 JSR PC,RANDAT ;R4=CRAM PC (LSB 8 BITS)
2884 016566 000125 125 ;EXPECTED DATA
2885 016570 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
2886 016572 001401 BEQ 6$ ;BR IF YES
2887 016574 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2888 016576 104405 6$: SCOPI ;LOOP TO 5$ IF SW59=1
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***** TEST 17 *****
*CRAM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
*SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION.
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC, AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37
*****

```

TEST 17

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2905 016600 000004 000017 001202 1$: SCOPE
2906 016602 012737 016764 001442 MOV #17,$STNM ; LOAD THE NO. OF THIS TEST
2907 016610 012737 016632 001444 MOV #T$20,NEXT ; POINT TO THE START OF NEXT TEST.
2908 016616 012737 016632 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
2909 ;R1 CONTAINS BASE KMC11 ADDRESS
2910 016624 104410 MSTCLR ;MASTER CLEAR KMC11
2911 016626 004737 021202 JSR PC,MEMSET ;SET MEM AND RAM
2912 016632 1$:
2913 016632 004737 021032 JSR PC,SETBRO ;SET THE BRO BIT'
2914 016636 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2915 016640 100400 100400 ;START AT ROM PC=0

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2916 016642 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2917 016644 116377 114377!(400*4) ;JUMP TO ROM PC OF 1777
2918 016646 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
2919 016652 000377 377 ;EXPECTED DATA
2920 016654 120504 CMPB RS,R4 ;IS ROM PC CORRECT?
2921 016656 001401 BEQ 2$ ;BR IF YES
2922 016660 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2923 016662 104405 SCOPI ;LOOP TO 1$ IF SW09=1
2924 016664 012737 016672 001444 MOV #3$,LOCK ;NEW SCOPI
2925 016672 004737 021032 JSR PC,SETBRO ;SET THE BRO BIT'
2926 016672 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2927 016676 100403 100403 ;START AT ROM PC=3
2928 016700 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2929 016702 102000 100000!(400*4) ;JUMP TO ROM PC OF 0
2930 016704 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
2931 016706 000000 0 ;EXPECTED DATA
2932 016712 120504 CMPB RS,R4 ;IS ROM PC CORRECT?
2933 016714 001401 BEQ 4$ ;BR IF YES
2934 016716 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2935 016720 104405 SCOPI ;LOOP TO 3$ IF SW09=1
2936 016722 012737 016732 001444 MOV #5$,LOCK ;NEW SCOPI
2937 016732 004737 021032 JSR PC,SETBRO ;SET THE BRO BIT'
2938 016736 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2939 016740 100406 100406 ;START AT ROM PC=6
2940 016742 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2941 016744 106125 104125!(400*4) ;JUMP TO ROM PC OF 525
2942 016746 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
2943 016752 000125 125 ;EXPECTED DATA
2944 016754 120504 CMPB RS,R4 ;IS ROM PC CORRECT?
2945 016756 001401 BEQ 6$ ;BR IF YES
2946 016760 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
2947 016762 104405 SCOPI ;LOOP TO 5$ IF SW59=1

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***** TEST 20 *****
*CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
*SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37
*****

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TEST 20

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2965 *****
2966 016764 000004 tST20: SCOPE ;*****
2967 016766 012737 000020 001202 MOV #20,$TSTNM ; LOAD THE NO. OF THIS TEST
2968 016774 012737 017150 001442 MOV #TST21,NEXT ; POINT TO THE START OF NEXT TEST.
2969 017002 012737 017016 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
2970 ;R1 CONTAINS BASE KMC11 ADDRESS
2971 017010 104410 MSTCLR ;MASTER CLEAR KMC11

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2972 017012 004737 021202          JSR    PC, MEMSET      ;SET MEM AND RAM
2973 017016          1$:          JSR    PC, SETBRI     ;SET THE BRI BIT'
2974 017016 004737 021040          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2975 017012 104412          100400 ;START AT ROM PC=0
2976 017024 100400          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2977 017026 104412          114377! <400*5> ;JUMP TO ROM PC OF 1777
2978 017030 116777          JSR    PC, RANDAT     ;R4=CRAM PC (LSB 8 BITS)
2979 017032 004737 021106          377      ;EXPECTED DATA
2980 017036 000377          CMPB   R5, R4         ;IS ROM PC CORRECT?
2981 017040 120504          BEQ    2$            ;BR IF YES
2982 017042 001401          ERROR  5            ;ERROR, CRAM PC IS WRONG
2983 017044 104005          SCOPI ;LOOP TO 1$ IF SW09=1
2984 017046 104405          MOV    #3$, LOCK    ;NEW SCOPI
2985 017050 012737 017056 001444 2$:
2986 017056          3$:          JSR    PC, SETBRI     ;SET THE BRI BIT'
2987 017056 004737 021040          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2988 017062 104412          100403 ;START AT ROM PC=3
2989 017064 100403          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2990 017066 104412          100000! <400*5> ;JUMP TO ROM PC OF 0
2991 017070 102400          JSR    PC, RANDAT     ;R4=CRAM PC (LSB 8 BITS)
2992 017072 004737 021106          0        ;EXPECTED DATA
2993 017076 000000          CMPB   R5, R4         ;IS ROM PC CORRECT?
2994 017100 120504          BEQ    4$            ;BR IF YES
2995 017102 001401          ERROR  5            ;ERROR, CRAM PC IS WRONG
2996 017104 104005          SCOPI ;LOOP TO 3$ IF SW09=1
2997 017106 104405          MOV    #5$, LOCK    ;NEW SCOPI
2998 017110 012737 017116 001444 4$:
2999 017116          5$:          JSR    PC, SETBRI     ;SET THE BRI BIT'
3000 017116 004737 021040          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3001 017122 104412          100406 ;START AT ROM PC=6
3002 017124 100406          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3003 017126 104412          104125! <400*5> ;JUMP TO ROM PC OF 525
3004 017130 106525          JSR    PC, RANDAT     ;R4=CRAM PC (LSB 8 BITS)
3005 017132 004737 021106          125      ;EXPECTED DATA
3006 017136 000125          CMPB   R5, R4         ;IS ROM PC CORRECT?
3007 017140 120504          BEQ    6$            ;BR IF YES
3008 017142 001401          ERROR  5            ;ERROR, CRAM PC IS WRONG
3009 017144 104005          SCOPI ;LOOP TO 5$ IF SW59=1
3010 017146 104405          6$:

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3012
3013 ;***** TEST 21 *****
3014 ;*CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
3015 ;*SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION.
3016 ;*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION.
3017 ;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
3018 ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3019 ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
3020 ;*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
3021 ;*THEN PORT4 WILL CONTAIN A 37
3022 ;*****
3023
3024 ; TEST 21
3025 ;-----
3026 ;*****
3027 017150 000004 †ST21: SCOPE

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3028 017152 012737 000021 001202      MOV      #21,$STSTNM      ; LOAD THE NO. OF THIS TEST
3029 017160 012737 017334 001442      MOV      #TST22,NEXT     ; POINT TO THE START OF NEXT TEST.
3030 017166 012737 017202 001444      MOV      #1$,LOCK        ; ADDRESS FOR LOCK ON DATA.
3031                                     ; R1 CONTAINS BASE KMC11 ADDRESS
3032 017174 104410                                     ; MASTER CLEAR KMC11
3033 017176 004737 021202      JSR      PC, MEMSET      ; SET MEM AND RAM
3034 017202                                     1$:
3035 017202 004737 021046      JSR      PC, SETBR4      ; SET THE BR4 BIT'
3036 017206 104412      ROMCLK   ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3037 017210 100400      ROMCLK   ; START AT ROM PC=0
3038 017212 104412      ROMCLK   ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3039 017214 117377      ROMCLK   ; JUMP TO ROM PC OF 1777
3040 017216 004737 021106      JSR      PC,RAMDAT      ; R4=CRAM PC (LSB 8 BITS)
3041 017222 000377      377      ; EXPECTED DATA
3042 017224 120504      CMPB     R5,R4          ; IS ROM PC CORRECT?
3043 017226 001401      BEQ      2$            ; BR IF YES
3044 017230 104005      ERROR    5            ; ERROR, CRAM PC IS WRONG
3045 017232 104405      SCOPI    ; LOOP TO 1$ IF SW09=1
3046 017234 012737 017242 001444      MOV      #3$,LOCK      ; NEW SCOPI
3047 017242                                     3$:
3048 017242 004737 021046      JSR      PC, SETBR4      ; SET THE BR4 BIT'
3049 017246 104412      ROMCLK   ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3050 017250 100403      ROMCLK   ; START AT ROM PC=3
3051 017252 104412      ROMCLK   ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3052 017254 103000      ROMCLK   ; JUMP TO ROM PC OF 0
3053 017256 004737 021106      JSR      PC,RAMDAT      ; R4=CRAM PC (LSB 8 BITS)
3054 017262 000000      0        ; EXPECTED DATA
3055 017264 120504      CMPB     R5,R4          ; IS ROM PC CORRECT?
3056 017266 001401      BEQ      4$            ; BR IF YES
3057 017270 104005      ERROR    5            ; ERROR, CRAM PC IS WRONG
3058 017272 104405      SCOPI    ; LOOP TO 3$ IF SW09=1
3059 017274 012737 017302 001444      MOV      #5$,LOCK      ; NEW SCOPI
3060 017302                                     5$:
3061 017302 004737 021046      JSR      PC, SETBR4      ; SET THE BR4 BIT'
3062 017306 104412      ROMCLK   ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3063 017310 100406      ROMCLK   ; START AT ROM PC=6
3064 017312 104412      ROMCLK   ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3065 017314 107125      ROMCLK   ; JUMP TO ROM PC OF 525
3066 017316 004737 021106      JSR      PC,RAMDAT      ; R4=CRAM PC (LSB 8 BITS)
3067 017322 000125      125      ; EXPECTED DATA
3068 017324 120504      CMPB     R5,R4          ; IS ROM PC CORRECT?
3069 017326 001401      BEQ      6$            ; BR IF YES
3070 017330 104005      ERROR    5            ; ERROR, CRAM PC IS WRONG
3071 017332 104405      SCOPI    ; LOOP TO 5$ IF SW59=1
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:***** TEST 22 *****
:*CRAM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
:*SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION.
:*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
:*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
:*THEN PORT4 WILL CONTAIN A 37
:*****

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3084
3085 ; TEST 22
3086 -----
3087 ;*****
3088 017334 000004 TST22: SCOPE
3089 017336 012737 000022 001202 MOV #22,STSTNM ; LOAD THE NO. OF THIS TEST
3090 017344 012737 017520 001442 MOV #TST23,NEXT ; POINT TO THE START OF NEXT TEST.
3091 017352 012737 017366 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
3092 ;
3093 017360 104410 ; R1 CONTAINS BASE KMC11 ADDRESS
3094 017362 004737 021202 MSTCLR ; MASTER CLEAR KMC11
3095 017366 ; JSR PC, MEMSET ; SET MEM AND RAM
3096 017366 004737 021054 1$: JSR PC, SETBR7 ; SET THE BR7 BIT'
3097 017372 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3098 017374 100400 100400 ; START AT ROM PC=0
3099 017376 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3100 017400 117777 114377! <400*7> ; JUMP TO ROM PC OF 1777
3101 017402 004737 021106 JSR PC, RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3102 017406 000377 377 ; EXPECTED DATA
3103 017410 120504 CMPB R5,R4 ; IS ROM PC CORRECT?
3104 017412 001401 BEQ 2$ ; BR IF YES
3105 017414 104005 ERROR 5 ; ERROR, CRAM PC IS WRONG
3106 017416 104405 2$: SCOP1 ; LOOP TO 1$ IF SW09=1
3107 017420 012737 017426 001444 MOV #3$,LOCK ; NEW SCOP1
3108 017426 3$:
3109 017426 004737 021054 JSR PC, SETBR7 ; SET THE BR7 BIT'
3110 017432 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3111 017434 100403 100403 ; START AT ROM PC=3
3112 017436 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3113 017440 103400 100000! <400*7> ; JUMP TO ROM PC OF 0
3114 017442 004737 021106 JSR PC, RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3115 017446 000000 0 ; EXPECTED DATA
3116 017450 120504 CMPB R5,R4 ; IS ROM PC CORRECT?
3117 017452 001401 BEQ 4$ ; BR IF YES
3118 017454 104005 ERROR 5 ; ERROR, CRAM PC IS WRONG
3119 017456 104405 4$: SCOP1 ; LOOP TO 3$ IF SW09=1
3120 017460 012737 017466 001444 MOV #5$,LOCK ; NEW SCOP1
3121 017466 5$:
3122 017466 004737 021054 JSR PC, SETBR7 ; SET THE BR7 BIT'
3123 017472 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3124 017474 100406 100406 ; START AT ROM PC=6
3125 017476 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3126 017500 107525 104125! <400*7> ; JUMP TO ROM PC OF 525
3127 017502 004737 021106 JSR PC, RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3128 017506 000125 125 ; EXPECTED DATA
3129 017510 120504 CMPB R5,R4 ; IS ROM PC CORRECT?
3130 017512 001401 BEQ 6$ ; BR IF YES
3131 017514 104005 ERROR 5 ; ERROR, CRAM PC IS WRONG
3132 017516 104405 6$: SCOP1 ; LOOP TO 5$ IF SW59=1
3133
3134
3135 ;***** TEST 23 *****
3136 ;*CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
3137 ;*CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,
3138 ;*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
3139 ;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE

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3140 ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3141 ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
3142 ;*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
3143 ;*THEN PORT4 CONTAINS A 37
3144 ;:*****
3145
3146 ; TEST 23
3147 ;-----
3148 ;:*****
3149 017520 000004 1ST23: SCOPE
3150 017522 012737 000023 001202 MOV #23,STSTNM ; LOAD THE NO. OF THIS TEST
3151 017530 012737 017704 001442 MOV #TST24,NEXT ; POINT TO THE START OF NEXT TEST.
3152 017536 012737 017552 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
3153 ;R1 CONTAINS BASE KMC11 ADDRESS
3154 017544 104410 MSTCLR ; MASTER CLEAR KMC11
3155 017546 004737 021202 JSR PC, MEMSET ; SET MEM AND RAM
3156 017552 1$: JSR PC, CLRALL ; CLEAR ALL CONDITIONS
3157 017552 004737 021014 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3158 017556 104412 100400 ; START AT ROM PC=0
3159 017560 100400 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3160 017562 104412 114377! <400*2> ; JUMP TO ROM PC OF 1777
3161 017564 115377 JSR PC, RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3162 017566 004737 021106 1 ; EXPECTED DATA
3163 017572 000001 CMPB R5,R4 ; IS ROM PC CORRECT?
3164 017574 120504 BEQ 2$ ; BR IF YES
3165 017576 001401 ERROR 5 ; ERROR, CRAM PC IS WRONG
3166 017600 104005 2$: SCOP1 ; LOOP TO 1$ IF SW09=1
3167 017602 104405 MOV #3$,LOCK ; NEW SCOP1
3168 017604 012737 017612 001444 3$: JSR PC, CLRALL ; CLEAR ALL CONDITIONS
3169 017612 004737 021014 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3170 017612 004737 021014 100403 ; START AT ROM PC=3
3171 017616 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3172 017620 100403 100000! <400*2> ; JUMP TO ROM PC OF 0
3173 017622 104412 JSR PC, RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3174 017624 101000 4 ; EXPECTED DATA
3175 017626 004737 021106 CMPB R5,R4 ; IS ROM PC CORRECT?
3176 017632 000004 4$ ; BR IF YES
3177 017634 120504 BEQ 4$ ; BR IF YES
3178 017636 001401 ERROR 5 ; ERROR, CRAM PC IS WRONG
3179 017640 104005 4$: SCOP1 ; LOOP TO 3$ IF SW09=1
3180 017642 104405 MOV #5$,LOCK ; NEW SCOP1
3181 017644 012737 017652 001444 5$: JSR PC, CLRALL ; CLEAR ALL CONDITIONS
3182 017652 004737 021014 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3183 017652 004737 021014 100406 ; START AT ROM PC=6
3184 017656 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3185 017660 100406 104125! <400*2> ; JUMP TO ROM PC OF 525
3186 017662 104412 JSR PC, RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3187 017664 105125 7 ; EXPECTED DATA
3188 017666 004737 021106 7 ; IS ROM PC CORRECT?
3189 017672 000007 CMPB R5,R4 ; BR IF YES
3190 017674 120504 BEQ 6$ ; BR IF YES
3191 017676 001401 ERROR 5 ; ERROR, CRAM PC IS WRONG
3192 017700 104005 6$: SCOP1 ; LOOP TO 5$ IF SW59=1
3193 017702 104405
3194
3195

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017704 000004  
017706 012737 000024 001202  
017714 012737 020070 001442  
017722 012737 017736 001444  
  
017730 104410  
017732 004737 021202  
017736  
017736 004737 021014  
017742 104412  
017744 100400  
017746 104412  
017750 115777  
017752 004737 021106  
017756 000001  
017760 120504  
017762 001401  
017764 104005  
017766 104405  
017770 012737 017776 001444  
017776  
017776 004737 021014  
020002 104412  
020004 100403  
020006 104412  
020010 101400  
020012 004737 021106  
020016 000004  
020020 120504  
020022 001401  
020024 104005  
020026 104405  
020030 012737 020036 001444  
020036  
020036 004737 021014  
020042 104412  
020044 100406  
020046 104412  
020050 105525  
020052 004737 021106  
020056 000007  
020060 120504

```
***** TEST 24 *****
*CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
*CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,
*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
*THEN PORT4 CONTAINS A 37
*****

TEST 24
-----
*****
1ST24: SCOPE
MOV #24,S1STNM ; LOAD THE NO. OF THIS TEST
MOV #1ST25,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1S,LOCK ; ADDRESS FOR LOCK ON DATA.

;R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
JSR PC,MEMSET ; SET MEM AND RAM

1S: JSR PC,CLRALL ; CLEAR ALL CONDITIONS
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100400 ; START AT ROM PC=0
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
114377!<400*3> ; JUMP TO ROM PC OF 1777
JSR PC,RAMDAT ; R4=CRAM PC (LSB 8 BITS)
1 ; EXPECTED DATA
CMPB R5,R4 ; IS ROM PC CORRECT?
BEQ 2S ; BR IF YES
ERROR 5 ; ERROR, CRAM PC IS WRONG
SCOPI ; LOOP TO 1S IF SW09=1
MOV #3S,LOCK ; NEW SCOPI

3S: JSR PC,CLRALL ; CLEAR ALL CONDITIONS
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100403 ; START AT ROM PC=3
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100000!<400*3> ; JUMP TO ROM PC OF 0
JSR PC,RAMDAT ; R4=CRAM PC (LSB 8 BITS)
4 ; EXPECTED DATA
CMPB R5,R4 ; IS ROM PC CORRECT?
BEQ 4S ; BR IF YES
ERROR 5 ; ERROR, CRAM PC IS WRONG
SCOPI ; LOOP TO 3S IF SW09=1
MOV #5S,LOCK ; NEW SCOPI

5S: JSR PC,CLRALL ; CLEAR ALL CONDITIONS
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100406 ; START AT ROM PC=6
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
104125!<400*3> ; JUMP TO ROM PC OF 525
JSR PC,RAMDAT ; R4=CRAM PC (LSB 8 BITS)
7 ; EXPECTED DATA
CMPB R5,R4 ; IS ROM PC CORRECT?
```

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3252 020062 001401      BEQ      6$      ; BR IF YES
3253 020064 104005      ERROR    5      ; ERROR, CRAM PC IS WRONG
3254 020066 104405      6$: SCOPI     ; LOOP TO 5$ IF SW59=1
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3271 020070 000004      ;*****
3272 020072 012737 000025 001202  †ST25: SCOPE
3273 020100 012737 020254 001442      MOV      #25,STSTNM      ; LOAD THE NO. OF THIS TEST
3274 020106 012737 020122 001444      MOV      #TST26,NEXT    ; POINT TO THE START OF NEXT TEST.
3275
3276 020114 104410      MOV      #15,LOCK      ; ADDRESS FOR LOCK ON DATA.
3277 020116 004737 021202      MSTCLR   ; R1 CONTAINS BASE KMC11 ADDRESS
3278 020122
3279 020122 004737 021014      JSR      PC,MEMSET     ; MASTER CLEAR KMC11
3280 020126 104412      JSR      PC,CLRALL    ; SET MEM AND RAM
3281 020130 100400
3282 020132 104412
3283 020134 116377
3284 020136 004737 021106      JSR      PC,CLRALL    ; CLEAR ALL CONDITIONS
3285 020142 000001      ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3286 020144 120504      100400  ; START AT ROM PC=0
3287 020146 001401      ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3288 020150 104005      114377!<400*4> ; JUMP TO ROM PC OF 1777
3289 020152 104405      JSR      PC,RAMDAT    ; R4=CRAM PC (LSB 8 BITS)
3290 020154 012737 020162 001444      1      ; EXPECTED DATA
3291 020162
3292 020162 004737 021014      CMPB    R5,R4        ; IS ROM PC CORRECT?
3293 020166 104412      BEQ      2$          ; BR IF YES
3294 020170 100403      ERROR    5          ; ERROR, CRAM PC IS WRONG
3295 020172 104412      2$: SCOPI         ; LOOP TO 1$ IF SW09=1
3296 020174 102000      MOV      #3$,LOCK    ; NEW SCOPI
3297 020176 004737 021106      3$: JSR      PC,CLRALL    ; CLEAR ALL CONDITIONS
3298 020202 000004      ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3299 020204 120504      100403  ; START AT ROM PC=3
3300 020206 001401      ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3301 020210 104005      100000!<400*4> ; JUMP TO ROM PC OF 0
3302 020212 104405      JSR      PC,RAMDAT    ; P4=CRAM PC (LSB 8 BITS)
3303 020214 012737 020222 001444      4      ; EXPECTED DATA
3304 020222
3305 020222 004737 021014      CMPB    R5,R4        ; IS ROM PC CORRECT?
3306 020226 104412      BEQ      4$          ; BR IF YES
3307 020230 100406      ERROR    5          ; ERROR, CRAM PC IS WRONG
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3333
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3308 020232 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3309 020234 106125 104125!(400*4) ;JUMP TO ROM PC OF 525
3310 020236 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3311 020242 000007 ;EXPECTED DATA
3312 020244 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
3313 020246 001401 BEQ 6$ ;BR IF YES
3314 020250 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
3315 020252 104405 6$: SCOPI ;LOOP TO 5$ IF SW9=1
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:***** TEST 26 *****
:*CRAM TEST OF JUMP(I) ON BRI SET MICRO-PROCESSOR INSTRUCTION.
:*CLEAR THE BRI BIT, PERFORM THE JUMP INSTRUCTION,
:*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
:*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
:*THEN PORT4 CONTAINS A 37
:*****

```

: TEST 26

```

3331
3332 020254 000004 1$T26: SCOPE
3333 020256 012737 000026 001202 MOV #26,$STNM ;LOAD THE NO. OF THIS TEST
3334 020264 012737 020440 001442 MOV #1$T27,NEXT ;POINT TO THE START OF NEXT TEST.
3335 020272 012737 020306 001444 MOV #1$,LOCK ;ADDRESS FOR LOCK ON DATA.
3336 ;R1 CONTAINS BASE KMC11 ADDRESS
3337 020300 104410 MSTCLR ;MASTER CLEAR KMC11
3338 020302 004737 021202 JSR PC,MEMSET ;SET MEM AND RAM
3339 020306 1$:
3340 020306 004737 021014 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
3341 020312 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3342 020314 100400 100400 ;START AT ROM PC=0
3343 020316 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3344 020320 116777 114377!(400*5) ;JUMP TO ROM PC OF 1777
3345 020322 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3346 020326 000001 ;EXPECTED DATA
3347 020330 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
3348 020332 001401 BEQ 2$ ;BR IF YES
3349 020334 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
3350 020336 104405 2$: SCOPI ;LOOP TO 1$ IF SW9=1
3351 020340 012737 020346 001444 MOV #3$,LOCK ;NEW SCOPI
3352 3$:
3353 020346 004737 021014 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
3354 020352 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3355 020354 100403 100403 ;START AT ROM PC=3
3356 020356 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3357 020360 102400 100000!(400*5) ;JUMP TO ROM PC OF 0
3358 020362 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3359 020366 000004 4 ;EXPECTED DATA
3360 020370 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
3361 020372 001401 BEQ 4$ ;BR IF YES
3362 020374 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
3363 020376 104405 4$: SCOPI ;LOOP TO 3$ IF SW9=1

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3364 020400 012737 020406 001444      5$:  MOV    #5$,LOCK      ;NEW SCOPI
3365 020406
3366 020406 004737 021014      JSR    PC,CLRALL      ;CLEAR ALL CONDITIONS
3367 020412 104412      ROMCLK                ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3368 020414 100406      100406                ;START AT ROM PC=6
3369 020416 104412      ROMCLK                ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3370 020420 106525      104125!<400*5>      ;JUMP TO ROM PC OF 525
3371 020422 004737 021106      JSR    PC,RAMDAT      ;R4=CRAM PC (LSB 8 BITS)
3372 020426 000007      7                      ;EXPECTED DATA
3373 020430 120504      CMPB   R5,R4          ;IS ROM PC CORRECT?
3374 020432 001401      BEQ    6$             ;BR IF YES
3375 020434 104005      ERROR  5              ;ERROR, CRAM PC IS WRONG
3376 020436 104405      6$:  SCOPI            ;LOOP TO 5$ IF SW59=1
3377
3378
3379

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:***** TEST 27 *****
:*CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
:*CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
:*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
:*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
:*THEN PORT4 CONTAINS A 37
:*****

```

: TEST 27

```

3392
3393 020440 000004      1$T27: SCOPE
3394 020442 012737 000027 001202      MOV    #27,$STNM      ; LOAD THE NO. OF THIS TEST
3395 020450 012737 020624 001442      MOV    #1$T30,NEXT    ; POINT TO THE START OF NEXT TEST.
3396 020456 012737 020472 001444      MOV    #1$,LOCK       ; ADDRESS FOR LOCK ON DATA.
3397
3398 020464 104410      MSTCLR
3399 020466 004737 021202      JSR    PC,MEMSET      ;R1 CONTAINS BASE KMC11 ADDRESS
3400 020472
3401 020472 004737 021014      1$:  JSR    PC,CLRALL      ;MASTER CLEAR KMC11
3402 020476 104412      ROMCLK                ;SET MEM AND RAM
3403 020500 100400      100400                ;CLEAR ALL CONDITIONS
3404 020502 104412      ROMCLK                ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3405 020504 117377      114377!<400*6>      ;START AT ROM PC=0
3406 020506 004737 021106      JSR    PC,RAMDAT      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3407 020512 000001      1                      ;JUMP TO ROM PC OF 1777
3408 020514 120504      CMPB   R5,R4          ;R4=CRAM PC (LSB 8 BITS)
3409 020516 001401      BEQ    2$             ;EXPECTED DATA
3410 020520 104005      ERROR  5              ;IS ROM PC CORRECT?
3411 020522 104405      2$:  SCOPI            ;BR IF YES
3412 020524 012737 020532 001444      MOV    #3$,LOCK       ;ERROR, CRAM PC IS WRONG
3413 020532
3414 020532 004737 021014      3$:  JSR    PC,CLRALL      ;LOOP TO 1$ IF SW09=1
3415 020536 104412      ROMCLK                ;NEW SCOPI
3416 020540 100403      100403                ;CLEAR ALL CONDITIONS
3417 020542 104412      ROMCLK                ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3418 020544 103000      100000!<400*E>      ;START AT ROM PC=3
3419 020546 004737 021106      JSR    PC,RAMDAT      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
                          ;JUMP TO ROM PC OF 0
                          ;R4=CRAM PC (LSB 8 BITS)

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3420 020552 000004 4 ; EXPECTED DATA
3421 020554 120504 CMPB R5,R4 ; IS ROM PC CORRECT?
3422 020556 001401 BEQ 4$ ; BR IF YES
3423 020560 104005 ERROR 5 ; ERROR, CRAM PC IS WRONG
3424 020562 104405 4$: SCOPI ; LOOP TO 3$ IF SW09=1
3425 020564 012737 020572 001444 MOV #5$,LOCK ; NEW SCOPI
3426 020572 5$:
3427 020572 004737 021014 JSR PC,CLRALL ; CLEAR ALL CONDITIONS
3428 020576 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3429 020600 100406 100406 ; START AT ROM PC=6
3430 020602 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3431 020604 107125 104125! <400*6> ; JUMP TO ROM PC OF 525
3432 020606 004737 021106 JSR PC,RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3433 020612 000007 7 ; EXPECTED DATA
3434 020614 120504 CMPB R5,R4 ; IS ROM PC CORRECT?
3435 020616 001401 BEQ 6$ ; BR IF YES
3436 020620 104005 ERROR 5 ; ERROR, CRAM PC IS WRONG
3437 020622 104405 6$: SCOPI ; LOOP TO 5$ IF SW59=1
3438
3439
3440 ; ***** TEST 30 *****
3441 ; *CRAM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
3442 ; *CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
3443 ; *VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
3444 ; *IN THE LOCATION IT IS AT, THIS INSTRUCTION LOADS THE
3445 ; *BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3446 ; *THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
3447 ; *THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
3448 ; *THEN PORT4 CONTAINS A 37
3449 ; *****
3450
3451 ; TEST 30
3452 ; -----
3453 ; *****
3454 020624 000004 1$T30: SCOPE
3455 020626 012737 000030 001202 MOV #30,$TSTNM ; LOAD THE NO. OF THIS TEST
3456 020634 012737 003662 001442 MOV #5EOP,NEXT ; POINT TO THE END OF PASS HANDLER.
3457 020642 012737 020656 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
3458 ; R1 CONTAINS BASE KMC11 ADDRESS
3459 020650 104410 MSTCLR ; MASTER CLEAR KMC11
3460 020652 004737 021202 JSR PC,MEMSET ; SET MEM AND RAM
3461 020656 1$:
3462 020656 004737 021014 JSR PC,CLRALL ; CLEAR ALL CONDITIONS
3463 020662 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3464 020664 100400 100400 ; START AT ROM PC=0
3465 020666 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3466 020670 117777 114377! <400*7> ; JUMP TO ROM PC OF 1777
3467 020672 004737 021106 JSR PC,RAMDAT ; R4=CRAM PC (LSB 8 BITS)
3468 020676 000001 1 ; EXPECTED DATA
3469 020700 120504 CMPB R5,R4 ; IS ROM PC CORRECT?
3470 020702 001401 BEQ 2$ ; BR IF YES
3471 020704 104005 ERROR 5 ; ERROR, CRAM PC IS WRONG
3472 020706 104405 2$: SCOPI ; LOOP TO 1$ IF SW09=1
3473 020710 012737 020716 001444 MOV #3$,LOCK ; NEW SCOPI
3474 020716 3$:
3475 020716 004737 021014 JSR PC,CLRALL ; CLEAR ALL CONDITIONS

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3476 020722 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3477 020724 100403 ;START AT ROM PC=3
3478 020726 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3479 020730 103400 100000! <400*7> ; JUMP TO ROM PC OF 0
3480 020732 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3481 020736 000004 4 ;EXPECTED DATA
3482 020740 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
3483 020742 001401 BEQ 4$ ;BR IF YES
3484 020744 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
3485 020746 104405 4$: SCOPI ;LOOP TO 3$ IF SW09=1
3486 020750 012737 020756 001444 MOV #5$,LOCK ;NEW SCOPI
3487 020756 5$:
3488 020756 004737 021014 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
3489 020762 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3490 020764 100406 100406 ;START AT ROM PC=6
3491 020766 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3492 020770 107525 104125! <400*7> ; JUMP TO ROM PC OF 525
3493 020772 004737 021106 JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3494 020776 000007 7 ;EXPECTED DATA
3495 021000 120504 CMPB R5,R4 ;IS ROM PC CORRECT?
3496 021002 001401 BEQ 6$ ;BR IF YES
3497 021004 104005 ERROR 5 ;ERROR, CRAM PC IS WRONG
3498 021006 104405 6$: SCOPI ;LOOP TO 5$ IF SW59=1
3499 021010 104420 ADVANCE ; ADVANCE TO NEXT TEST
3500
3501
3502
3503 ; BUFFER AREA
3504 ;-----
3505
3506 021012 000000 FLAG: 0
3507
3508
3509 ; SUBROUTINES
3510 ;-----
3511
3512 021014 CLRALL:
3513 ; THIS SUBROUTINE CLEARS THE C&Z BITS AND THE BR
3514
3515 021014 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3516 021016 000400 000400 ;BR+0
3517 021020 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3518 021022 063220 063220 ;SP(0)+BR
3519 021024 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3520 021026 060400 060400 ;BR+SP(0)+BR
3521 021030 000207 RTS PC
3522
3523
3524 021032 SETBRO:
3525 ; THIS SUBROUTINE SETS BRO BIT
3526
3527 021032 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3528 021034 000401 000401 ;BR+001
3529 021036 000207 RTS PC
3530
3531
    
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3532 021040          SETBR1:
3533                    ;THIS SUBROUTINE SETS BR1 BIT
3534
3535 021040 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3536 021042 000402    000402          ;BR+002
3537 021044 000207    RTS          PC
3538
3539
3540 021046          SETBR4:
3541                    ;THIS SUBROUTINE SETS BR4 BIT
3542
3543 021046 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3544 021050 000420    000420          ;BR+020
3545 021052 000207    RTS          PC
3546
3547
3548 021054          SETBR7:
3549                    ;THIS SUBROUTINE SETS BR7 BIT
3550
3551 021054 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3552 021056 000600    000600          ;BR+200
3553 021060 000207    RTS          PC
3554
3555
3556 021062          SETC:
3557                    ;THIS SUBROUTINE SETS THE C BIT
3558
3559 021062 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3560 021064 000777    000777          ;BR+377
3561 021066 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3562 021070 063220    063220          ;SP(0)+BR
3563 021072 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3564 021074 060400    060400          ;BR+SP(0)+BR
3565 021076 000207    RTS          PC
3566
3567
3568 021100          SETZ:
3569                    ;THIS SUBROUTINE SETS THE Z BIT
3570
3571 021100 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3572 021102 000777    000777          ;BR+377
3573 021104 000207    RTS          PC
3574
3575
3576 021106          RAMDAT:
3577                    ;THIS SUBROUTINE LOADS R4 WITH THE LOWEST
3578                    ;8 BITS OF THE CRAM PC.
3579
3580 021106 017605 000000    MOV      2(SP),R5      ;GOOD DATA
3581 021112 062716 000002    ADD      #2(SP)      ;ADJUST STACK
3582 021116 005011          CLR      (R1)        ;CLEAR BIT10
3583 021120 052711 000400    BIS      #BIT8,(R1)  ;CLOCK INSTRUCTION IN CRAM THAT WAS
3584                    ;JUMPED TO, IT LOADS BR WITH ROM PC
3585 021124 005011          CLR      (R1)        ;CLR BIT8
3586 021126 104412    ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3587 021130 061225    061225          ;MOV BR TO PORT 5

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3588 021132 116104 000005      MOVB 5(R1),R4      ;PUT "FOUND" IN R4
3589 021136 000207              RTS PC             ;RETURN
3590
3591 021140                      WROM:
3592                      ;THIS SUBROUTINE WRITES THE ROMMAP INTO THE CRAM
3593
3594                      ;
3595                      ; BIT #BIT15,STAT1 ;BE SURE KMC HAS CRAM
3596                      ; BEQ 2$          ;SKIP IF NO CRAM
3597 021140 005000              CLR R0            ;R0=CRAM ADDRESS
3598 021142 012702 013732      MOV #ROMMAP,R2    ;R2 POINTS TO ROMMAP
3599 021146 012711 002000      1$: MOV #BIT10,(R1) ;SET ROMO
3600 021152 010061 000004      MOV R0,4(R1)      ;LOAD CRAM ADDRESS
3601 021156 012261 000006      MOV (R2)+,6(R1)   ;LOAD WORD TO BE WRITTEN
3602 021162 052711 020000      BIS #BIT13,(R1)  ;WRITE IT!
3603 021166 005200              INC R0            ;NEXT ADDRESS
3604 021170 022700 002000      CMP #2000,R0     ;DONE YET?
3605 021174 001364              BNE 1$           ;BR IF NO
3606 021176 005011              CLR (R1)         ;CLEAR SELD
3607 021200 000207              RTS PC             ;RETURN
3608
3609 021202                      MEMSET:
3610                      ;THIS SUBROUTINE LOADS CRAM WITH SPECIAL INSTRUCTIONS
3611                      ;FOR THE CRAM JUMP TEST. ALL CRAM LOCATIONS ARE LOADED
3612                      ;WITH INSTRUCTIONS THAT MOVE A 37 TO THE BR, EXCEPT THE
3613                      ;FOLLOWING CRAM ADDRESSES: 0,1,4,7,525,1777. THESE LOCATIONS
3614                      ;CONTAIN INSTRUCTIONS WHICH LOAD THE BR WITH THE LOWEST
3615                      ;8 BITS OF THAT CRAM ADDRESS.
3616
3617 021202 005000              CLR R0            ;R0 = CRAM ADDRESS
3618 021204 012711 002000      1$: MOV #BIT10,(R1)  ;SET ROMO
3619 021210 010061 000004      MOV R0,4(R1)      ;LOAD CRAM ADDRESS
3620 021214 012761 000437 000006  MOV #437,6(R1)    ;LOAD INSTRUCTION
3621 021222 052711 020000      BIS #BIT13,(R1)  ;WRITE INSTRUCTION IN CRAM
3622 021226 005200              INC R0            ;NEXT ADDRESS
3623 021230 022700 002000      CMP #2000,R0     ;DONE YET?
3624 021234 001363              BNE 1$           ;BR IF NO
3625 021236 005000              CLR R0            ;INDEX REGISTER
3626 021240 012711 002000      2$: MOV #BIT10,(R1)  ;SET ROMO
3627 021244 016061 021300 000004  MOV CRAMA(R0),4(R1) ;LOAD CRAM ADDRESS IN SEL4
3628 021252 016061 021314 000006  MOV INSTU(R0),6(R1) ;LOAD INSTRUCTION TO BE WRITTEN
3629 021258 052711 020000      BIS #BIT13,(R1)  ;WRITE CRAM!
3630 021264 005720              TST (R0)+        ;NEXT
3631 021266 022700 000014      CMP #14,R0       ;DONE YET?
3632 021272 001362              BNE 2$           ;BR IF NO
3633 021274 005011              CLR (R1)         ;CLEAR ALL BITS
3634 021276 000207              RTS PC             ;RETURN
3635
3636 021300 000000 000001 000004  CRAMA: .WORD 0,1,4,7,1777,525
3637 021306 000007 001777 000525
3638 021314 000400          INSTU: 000400 ;BR+0
3639 021316 000401          ;000401 ;BR+1
3640 021320 000404          ;000404 ;BR+4
3641 021322 000407          ;000407 ;BR+7
3642 021324 000777          ;000777 ;BR+377
3643 021326 000525          ;000525 ;BR+125
    
```

3644  
3645  
3646

021330	041600	040522	020115	EM1:	.ASCIZ	<200>/CRAM DATA ERROR/
021351	200	051103	046501	EM2:	.ASCIZ	<200>/CRAM DUAL ADDRESSING ERROR/
021405	200	052512	050115	EM3:	.ASCIZ	<200>/JUMP ERROR/
021421	200	042117	020124	EM4:	.ASCIZ	<200>/OOT ERROR IN IBUS* REG10/
021453	200	047511	020120	EM5:	.ASCIZ	<200>/IOP MAIN MEMORY TEST/
021501	200	047511	020120	EM6:	.ASCIZ	<200>/IOP MAR TEST/
021517	200	051102	051040	EM7:	.ASCIZ	<200>/BR RIGHT SHIFT TEST/

021544	042600	050130	041505	DH1:	.ASCIZ	<200>/EXPECTED FOUND ADDRESS/
021576	042600	050130	041505	DH2:	.ASCIZ	<200>/EXPECTED FOUND/
	021620			.EVEN		

021620	000003			DT1:	3	
021622	006	004		.BYTE		6,4
021624	001266			\$REG2		
021626	006	004		.BYTE		6,4
021630	001272			\$REG4		
021632	004	002		.BYTE		4,2
021634	001262			\$REG0		
021636	000003			DT2:	3	
021640	006	004		.BYTE		6,4
021642	001274			\$REG5		
021644	006	004		.BYTE		6,4
021646	001272			\$REG4		
021650	004	002		.BYTE		4,2
021652	001266			\$REG2		
021654	000002			DT3:	2	
021656	003	007		.BYTE		3,7
021660	001274			\$REG5		
021662	003	002		.BYTE		3,2
021664	001272			\$REG4		
021666	000003			DT4:	3	
021670	003	010		.BYTE		3,10
021672	001274			\$REG5		
021674	003	004		.BYTE		3,4
021676	001272			\$REG4		
021700	004	002		.BYTE		4,2
021702	021012			FLAG		
021704	000003			DT5:	3	
021706	003	010		.BYTE		3,10
021710	001274			\$REG5		
021712	003	004		.BYTE		3,4
021714	001272			\$REG4		
021716	004	002		.BYTE		4,2
021720	001266			\$REG2		

021722	000001			CORMAX:		
				.END		

ABASE = 000000	268	309		
ACOM1 = 000000	268	311		
ACOM2 = 000000	268	312		
ACPUOP = 000000	268	283		
ADWD = 000000	268	313		
ADW1 = 000000	268	314		
ADW10 = 000000	268	323		
ADW11 = 000000	268	324		
ADW12 = 000000	268	325		
ADW13 = 000000	268	326		
ADW14 = 000000	268	327		
ADW15 = 000000	268	328		
ADW2 = 000000	268	315		
ADW3 = 000000	268	316		
ADW4 = 000000	268	317		
ADW5 = 000000	268	318		
ADW6 = 000000	268	319		
ADW7 = 000000	268	320		
ADW8 = 000000	268	321		
ADW9 = 000000	268	322		
ADEVCT = 000000	268	274		
ADEVN = 000000	268	310		
ADRCNT 006057	1334*	1349*	1358#	
ADVANC= 104420	1503#	3499		
RENV = 000002	1#	268	279	
REVM = 000000	268	280		
AFATAL = 000000	268	271		
AMDR1 = 000000	268	296		
AMDR2 = 000000	268	300		
AMDR3 = 000000	268	303		
AMDR4 = 000000	268	306		
AMMS1 = 000000	268	290		
AMMS2 = 000000	268	298		
AMMS3 = 000000	268	301		
AMMS4 = 000000	268	304		
AMSGAD = 000000	268	276		
AMSGLC = 000000	268	277		
AMSGTY = 000000	268	270		
AMTYP1 = 000000	268	291		
AMTYP2 = 000000	268	299		
AMTYP3 = 000000	268	302		
AMTYP4 = 000000	268	305		
APASS = 000000	268	273		
APRIOR = 000000	268			
APTCSU = 000040	1059	1164#		
APTENV = 000001	1052	1120	1162#	1564
APTSIZ = 000200	1161#			
APTSPO = 000100	1054	1122	1163#	
APT.SI 013510	727	2138#		
ASWREG = 000000	268	281		
ATESTN = 000000	268	272		
AUDONE 003354	764	785	824#	
AUNIT = 000000	268	275		
AUSTRT 003126	763#			
AUSWR = 000000	268	282		
AUTO.S 012110	725	1882#		











DZKCD.P11 21-MAR-77 17:24 CROSS REFERENCE TABLE -- USER SYMBOLS

MERR3	007672	834	1703#											
MILK	001504	357#	671#	910	1803*	1808*	1812							
MLOCK	007716	875	1703#											
MNEW	010017	829	1703#											
MODU	010461	1703#	1943											
MPASSX	007761	906	1703#											
MPFAIL	007562	1621	1638	1703#										
MR	007642	882	1703#	1860										
MRESET=	004000	159#												
MSTCLR=	104410	1495#	1627	2204	2280	2318	2365	2400	2446	2495	2562	2604	2669	2730
		2788	2849	2910	2971	3032	3093	3154	3215	3276	3337	3398	3459	
MTITLE	001000	207#	702											
MTSTN	010003	1544	1703#	1845										
MVECX	007753	904	1703#											
NEXT	001442	336#	1363	1583	2202*	2243*	2277*	2315*	2362*	2397*	2443*	2492*	2560*	2601*
		2666*	2727*	2785*	2846*	2907*	2968*	3029*	3090*	3151*	3212*	3273*	3334*	3395*
		3456*												
NOACT	010731	714	1703#	1797										
NODEV	003240	765	787#											
NUM	010323	1703#	1896											
OK	003220	779	782#	805										
ONE	001464	348#												
PACT00	002302	553#												
PACT01	002306	556#												
PACT02	002312	559#												
PACT03	002316	562#												
PACT04	002322	565#												
PACT05	002326	568#												
PACT06	002332	571#												
PACT07	002336	574#												
PACT10	002342	577#												
PACT11	002346	580#												
PACT12	002352	583#												
PACT13	002356	586#												
PACT14	002362	589#												
PACT15	002366	592#												
PACT16	002372	595#												
PACT17	002376	598#												
PARBIT=	040000	159#												
PERFOR=	004537	159#												
PFTAB	007324	1622	1644#											
PIRQ =	177772	49#												
FIRQVE=	000240	143#												
POPRO =	012600	154#	1577											
POP1SP=	005726	152#												
POP2SP=	022626	156#												
PRI0	010422	1703#	1924											
PRIATY	013730	2145*	2151*	2164	2185#									
PRO =	000000	66#	2121	2122										
PR1 =	000040	67#												
PR2 =	000100	68#												
PR3 =	000140	69#												
PR4 =	000200	70#	2123											
PR5 =	000240	71#	2124											
PR6 =	000300	72#	2125											
PR7 =	000340	73#	178	180	182	184	2126							





















SSSKIP	1448	
.EQUAT	18	34
.HEADE	18	
.SETUP	18	
.SACT1	18	185
.SAPT8	18	2658
.SAPTH	18	412
.SAPTY	18	1108
.SCATC	18	
.SCHTA	18	210
.SEOP	18	890
.SERRO	18	
.SERRT	18	
.SPOWE	18	1596
.SROOC	18	1270
.SREAO	18	1167
.SSCOP	18	957
.STRAP	18	1455
.STYPE	18	1029
.STYPO	18	

. ABS. 021722 000

ERRORS DETECTED: 0  
DEFAULT GLOBALS GENERATED: 0

DZKCD,DZKCD/SOL/CRF+DZKCD.MAC,DZKCD.P11/EQ:DZDMG  
RUN-TIME: 25 19 1 SECONDS  
RUN-TIME RATIO: 82/46=1.7  
CORE USED: 51k (102 PAGES)

EOF1DZKCDASEQ

00C100C0

770720

PDP10 411